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Bacheloroppgave

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3-phase DC/AC converter with SV-PWM

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Bachelor of Science in Electric Power Engineering
Submission date: May 2023
Supervisor: Eirik Haustveit

Western Norway University of Applied Sciences
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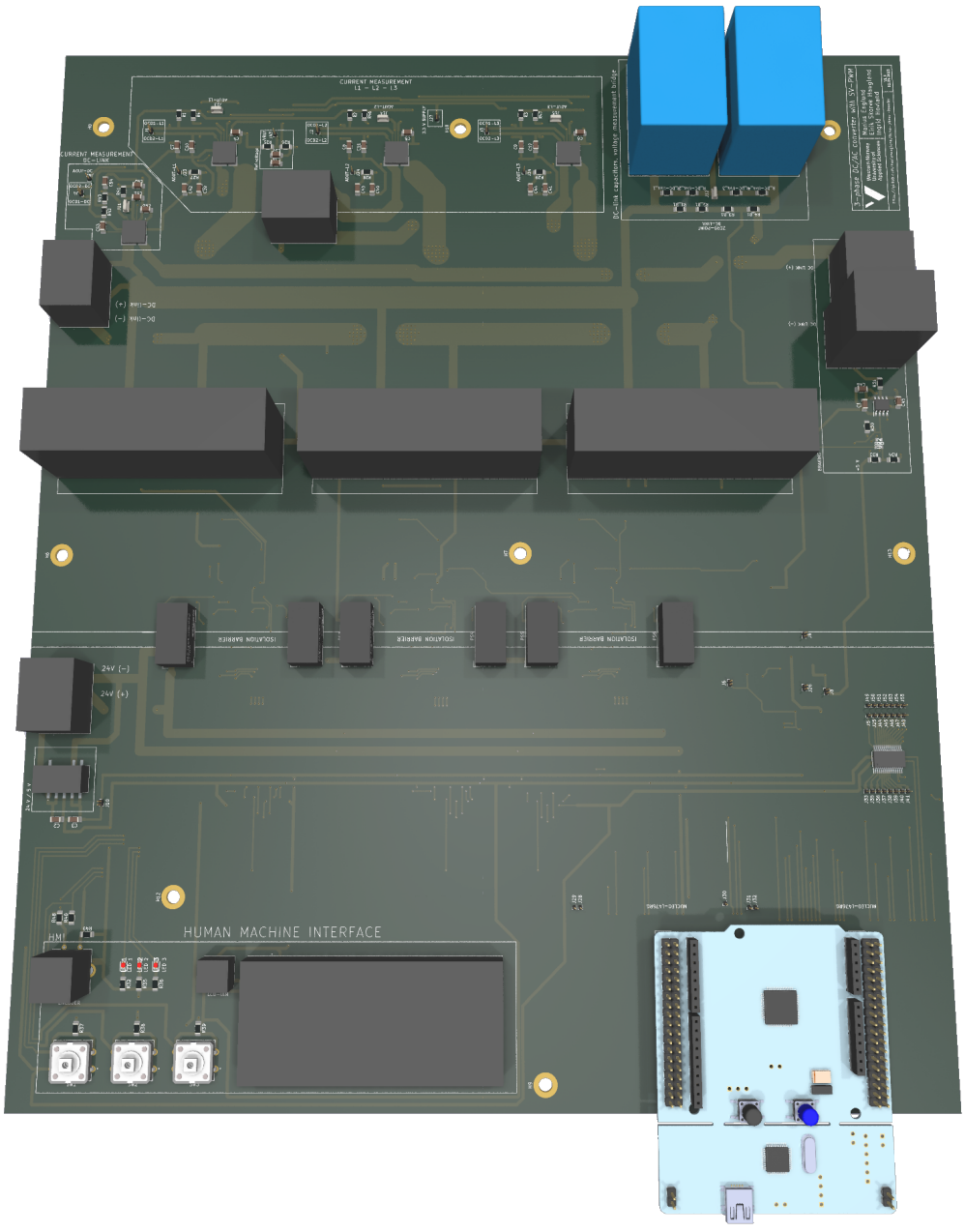

A DC-to-AC converter development project.

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Preface

This project, titled "3-phase DC/AC converter with SV-PWM", was conducted at the Western Norway University of Applied Sciences (HVL), Department of Computer Science, Electrical Engineering and Mathematical Sciences during the spring semester of 2023.

As the authors of this thesis, we are pleased to present the culmination of our academic journey towards obtaining a Bachelor's degree in Electric Power Engineering. The project was initiated by a lecture we attended during the fall semester of 2022, which presented a compelling topic that sparked our interest.

Over the course of several months, we have dedicated ourselves to research, experimentation, and analysis in order to develop a comprehensive understanding of power converter technologies and their applications in the contemporary power industry. It has been a challenging undertaking, but we were motivated to ensure that our objectives were met.

We hope that this report will serve as a valuable resource for those who are interested in the field, and we encourage further development of the provided resources.

Despite utilizing tools to improve the academic tone of the report, we unequivocally declare that this thesis, along with the research presented within it, are entirely original and the result of our own efforts.

Bergen, 22 May 2023

Marius Englund	Eirik Skorve Haugland	Ingrid Hovland

Acknowledgements

We offer our profound appreciation to our supervisor, Eirik Haustveit, for your outstanding efforts in assisting and guiding us throughout the course of the project. Your dedication and mastery of the subject matter have been invaluable in ensuring the successful completion of our work.

Additionally, we would like to acknowledge Vegard Steinsland for your valuable advice during the project, as well as the generous loan of your rectifier. We would also like to thank Farzan Jouleh for your assistance in procuring the necessary components, and Endre Håland for your help in ordering the circuit board.

Furthermore, we wish to express our gratitude to the faculty and lecturers at HVL for providing us with a challenging yet rewarding academic environment. This has enabled us to navigate the complexities of our chosen field.

Lastly, we want to recognize our classmates at HVL for the experiences we have shared together over the past three years. We wish you all the best as you embark on the next chapter of your careers.

M. Englund
E. S. Haugland
I. Hovland

Abstract

Electric motors are indispensable in modern industries and are utilized in a wide range of applications that impact various aspects of our daily lives. Motor drives are responsible for nearly two-thirds of the world's total energy consumption, highlighting the importance of developing energy-efficient control techniques. Pulse Width Modulation (PWM) enable the regulation of speed and torque of AC machines and can contribute significantly to the energy efficiency of motor applications. This bachelor's thesis presents the development of a three-phase two-level DC-to-AC converter that utilizes Space Vector Pulse Width Modulation (SV-PWM) to control the induction machine.

The work presented in the thesis investigates the interdependence between theoretical principles of motor control and circuit board design, encompassing aspects such as components selection, code development, and simulation. An essential aspect of the project involves developing a quality control method to ensure the circuit board's reliability and functionality. Laboratory experiments are conducted to evaluate the design's effectiveness in real-world scenarios, comparing two modulation techniques while the circuit board is connected to both resistive and inductive loads.

After conducting a series of tests on the converter with the aim of resolving issues and enhancing its design, the outcomes have demonstrated a circuit board that is operational and adheres to its specified functional description. The laboratory experiments confirmed the correspondence between theory and practice, and verified the converter's ability to control the induction machine. In line with the employer's requirements, the results indicate that the design is suitable for use in future educational laboratory experiments.

To augment the converter's usefulness as an educational tool, it is advisable to implement

multiple modulation algorithms and examine compatibility with other motor categories. A major expansion could involve making the converter bidirectional, allowing for power conversion in generator operation. For further details, please refer to the chapter on *Suggestions for Further Work*.

Keywords: Space Vector Pulse Width Modulation, SV-PWM, Sinusoidal Pulse Width Modulation, SPWM, inverter, PCB design, motor drives

Samandrag

Elektriske motorar har ei avgjerande rolle i moderne industri og vert brukt i eit breitt spekter av applikasjonar som påverkar ulike aspekt av kvardagen vår. Motordrifter er ansvarlege for nærmare to tredjedelar av verdas totale energiforbruk, noko som understrekar viktigheita av å utvikle energieffektive teknikkar for å styre dei. Pulsbreiddemodulasjon (PWM) gjer det mogleg å regulere både hastigheita og dreiemomentet til vekselstraumsmaskiner, og kan dermed bidra til å energieffektivisere motorapplikasjonar. Denne bacheloroppgåva presenterer utviklinga av ein trefasa tonivå likestraum-til-vekselstraum-omformar som nyttar romvektormodulasjon (SV-PWM) for å kontrollere induksjonsmaskina.

Arbeidet som presenterast i oppgåva utforskar samanhengen mellom teoretiske prinsipp for motorstyring og krinskortdesign, inkludert prosessar som val av komponentar, kodeutvikling og simulering. Ein viktig del av prosjektet involverer utviklinga av ein kvalitetskontrollmetode for å sikre pålitelegheit og funksjonalitet til krinskortet. Laboratorieeksperiment blir utførte for å evaluere effektiviteten til designet i reelle situasjonar, der to ulike modulasjonsteknikkar blir samanlikna medan krinskortet er tilkopla både resistiv og induktiv belastning.

Etter å ha gjennomført ei rekkje testar på omformaren med mål om å rette feil og forbetre designet, viste resultata eit fungerande krinskort som oppfylte si angitte funksjonsbeskriving. Laboratorieforsøka stadfesta samsvaret mellom teori og praksis, og verifiserte omformarens evne til å styre induksjonsmaskina. I tråd med oppdragsgjevarens ynskjer, fastslår resultata at designet eigna seg for bruk i framtidige utdanningsrelaterte laboratorieeksperiment.

For å auke nytteverdien av omformaren som eit opplæringsverktøy, ville det vere føremålstenleg å implementere fleire modulasjonsalgoritmar, samt undersøkje kompatibiliteten

med andre motorkategoriar. Ei større utviding kan vere å gjere omformaren støttande for effektflyt i begge retningar, slik at den også kan brukast som kraftomformar i generatordrift. For fleire detaljar visast det til kapittelet om *Forslag til Vidare Arbeid*.

Nøkkelord: romvektormodulasjon, SV-PWM, sinusforma pulsbreiddemodulasjon, SPWM, vekselomformar, krinskortdesign, motordrifter

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Introduction

According to global energy consumption statistics, nearly two-thirds of the energy used worldwide is consumed by motor drives [7, p. xi], with induction motors accounting for 80 % of the energy [17]. Induction motors, also referred to as asynchronous motors, are highly efficient electrical machines that convert electrical energy into mechanical energy. Their reliability and simple construction have made them the most commonly used electric motor in the world, being employed in a wide range of applications, from household appliances to industrial systems. In recent years, the induction motor has also gained significant market share in mobile applications, such as electric vehicles [7, p. 3-4].

Background

The induction motor comprises a stationary part known as the stator and a rotating part known as the rotor. Its operation relies on the principle of electromagnetic induction, which states that a magnetic field can induce an electrical current in a nearby conductor. In the case of induction motors, such a magnetic field is generated by passing an alternating current (AC) through the stator windings. This induces a current in the rotor windings, causing the rotor shaft to rotate [7, p. 194-199]. To achieve optimal efficiency, precise control of the rotor speed and torque is essential. The amplitude and frequency of the stator voltage are the primary determinants of these parameters and can be adjusted using a Power Processing Unit (PPU).

A common approach to power processing involves rectifying the alternating power supply into direct current (DC) and subsequently utilizing modulation techniques, such as Pulse

Width Modulation (PWM), to reconvert it to AC waveforms with the appropriate voltage and frequency. An electronic device known as an inverter is central in enabling this conversion, working by switching the DC voltage on and off at high frequencies to generate sinusoidal waveforms with the desired characteristics.

Project Overview

The aim of this project is to design and fabricate a two-level inverter that utilizes the Space Vector Pulse Width Modulation (SV-PWM) algorithm to generate a three-phase alternating current from a direct current source, thereby enabling the control of induction motors. The finalized circuit design, together with its associated research, will serve as a learning resource in future laboratory exercises at Western Norway University of Applied Sciences.

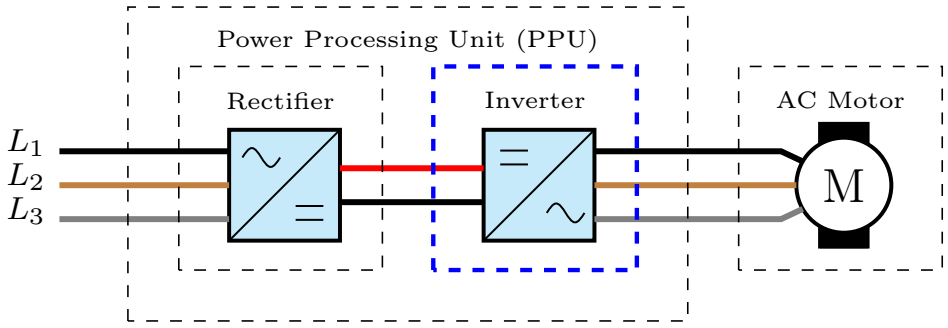


Figure 1: The circuitry to be fabricated.
Source: Created using CircuiTikZ.

In Figure 1, the delineated section highlighted by the blue dashed line represents the specific circuitry to be fabricated within the context of a Power Processing Unit.

Employer

Western Norway University of Applied Sciences, also known as HVL, is a highly esteemed institution of higher education located in Norway and serves as the commissioning body

for the present project. As one of the largest universities in the country, HVL covers a total of 17 000 students and 1750 staffs. The university is comprised of four faculties, each of which offers a diverse range of undergraduate and graduate programs. The faculties span the fields of health and social sciences, education, culture and sports, engineering and natural sciences, economics and social sciences. Annually HVL graduates approximately 4500 candidates [10].

Structure of the Report

This chapter has introduced the induction machine and the inverter, along with a presentation of the project's objective and employer. Moving forward, the report is divided into three parts, each focusing on a specific aspect of the project.

The initial part explores the induction machine, including various control methodologies and the challenges associated with inverter design. Moreover, it delves into the theoretical principles of different modulation techniques and the respective strengths and limitations of each. This section establishes the fundamental basis for the subsequent design development.

The second part is dedicated to the design process, which begins with an assessment of the demands and specifications that must be incorporated into the design. Following this, a comprehensive exposition of the design process is provided, with due consideration given to various design factors that are critical for achieving the desired outcomes.

The third part is primarily focused on practical verification of the design through laboratory experiments. It presents an overview of the methodology used in these experiments, along with an analysis of the results.

In conclusion, the report summarizes the three parts and evaluates the finalized design. The report also suggests areas for **further improvement** in future work.

Additionally, **the appendices** comprise of supplementary details on project management and helpful resources for potential future contributions. These encompass a range of materials, including 3D models, PCB layout, circuit diagrams, identified design flaws,

program code, simulation results and a laboratory exercise for educational purposes.

Part I

Theory

Chapter 1

Induction Machines and Operation

As asserted in the introductory chapter, the induction machine holds a prominent position as the most widely used electric motor worldwide. This popularity stems from the machine's ability to maintain a nearly constant speed under constant voltage and frequency [7, p. 193]. Nevertheless, to effectively regulate the speed and torque, it is imperative to grasp the operational principles of the machine. The three-phase induction machine is built upon a simple structure of three stator windings that are mutually displaced in space by 120 degrees. Upon supplying these windings with current, a magnetic field is generated and utilized in the rotor to rotate a shaft, which is usually connected to a mechanical load. This chapter aims to introduce the construction of the machine, elucidate some methods of controlling its speed and torque, and also examines the underlying principles governing its operation as a generator, which is crucial in inverter design.

1.1 Electrical Model

It is essential to examine the equivalent circuit depicted in Figure 1.1 to gain a thorough understanding of the induction motor. Through the use of the equivalent circuit, which is based on a wye connection for the stator and rotor, each winding can be visualized for each phase. Such a comprehensive overview provides insight into the multifarious parameters that influence the motor [4, p. 330].

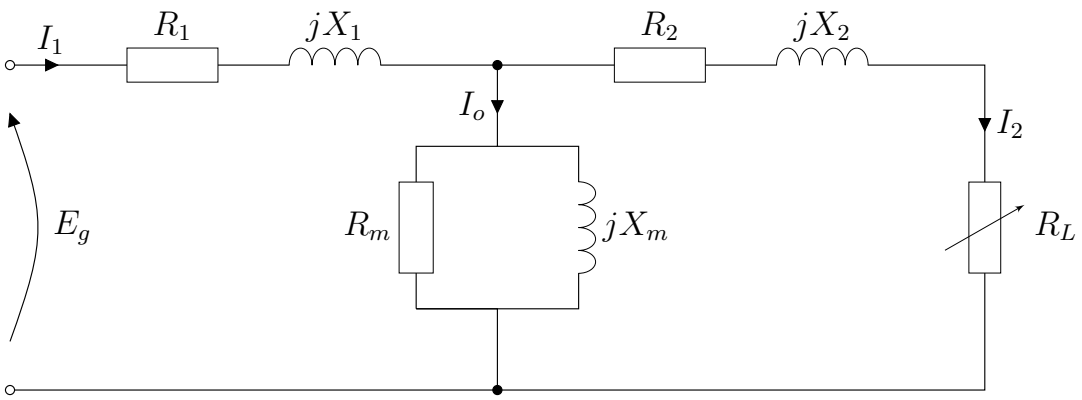


Figure 1.1: The equivalent circuit of an induction motor at standstill.
Source: Created using CircuiTikZ.

The left-hand side of the equivalent circuit visualizes the phase voltage, E_g, that is connected to the stator windings. The stator comprises a winding resistance, R_1, and a leakage reactance, jX_1, while the current flowing through them represents the line current, I_1. These parameters are important for modeling the behavior of the induction machine under different operating conditions, such as varying loads or frequency [4, p. 273].

In the middle of the equivalent circuit, the magnetizing resistance, R_m, and magnetizing reactance, jX_m, form a magnetizing branch with the corresponding magnetizing current, I_o. The electrical losses in R_m corresponds directly to iron, windage and friction losses in the motor, while the value of jX_m affects the reactive power generated by the motor.

On the right-hand side, the rotor is illustrated, comprising a winding resistance, R_2, and a leakage reactance, jX_2. These parameters are important in determining the motor's starting and running performance, as well as its efficiency [4, p. 264].

The output is illustrated with a variable resistive load, R_L, allowing the regulation of the motor's load current, I_2. This change in current can affect the torque produced by the motor, which in turn can impact its speed and efficiency. The effective connection between one slip-ring and the neutral of the rotor is established through the presence of R_L [4, p. 331-332].

1.2 Speed and Torque Control

One of the most significant benefits of Variable Frequency Drive (VFD) is their ability to achieve the same level of torque without any increase in current. This is due to the VFD's ability to adjust the frequency of the voltage supplied to the motor, which in turn controls the speed of the motor. By adjusting the frequency of the voltage, VFD's can vary the amount of power supplied to the motor, allowing the motor to operate at the desired speed and torque with minimal energy consumption [4, p. 471-474]. The relationship between speed and torque developed in a motor is often visualized using a torque-speed curve as demonstrated in Figure 1.2.

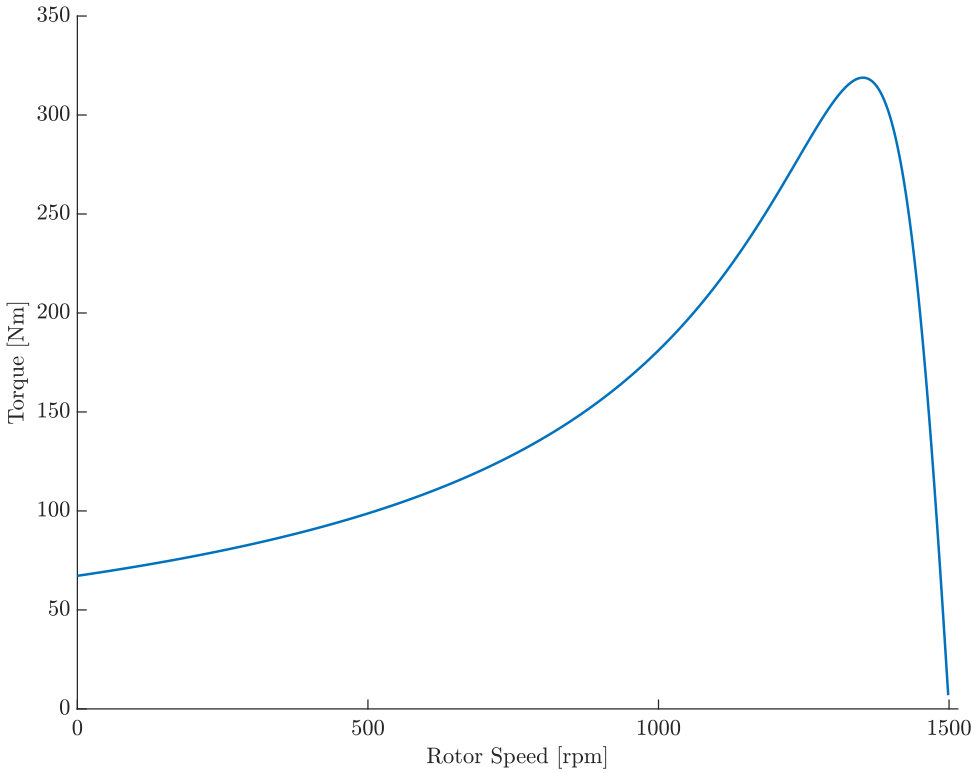


Figure 1.2: Typical torque-speed curve of an induction motor operated at fixed voltage and frequency.
Source: Created using MATLAB.

Constant U/f

Scalar control, also known as constant U/f, is a commonly used method to control the speed and torque in variable frequency drives. The method involves a modulator for proportionally varying the amplitude and frequency of the voltage applied to the stator windings, which enables the motor to deliver maximum rated torque while keeping frequency, rotor current, and stator current within rated values. However, varying mechanical loads may affect the accuracy of the output due to motor slip. When the operating frequency of the motor falls below approximately 20 % of its rated frequency, f_n, it becomes necessary to progressively increase the volts-per-hertz ratio to offset the voltage drop resulting from the resistance of the stator windings [4, p. 472]. Scalar control is recognized as a technically uncomplicated and cost-effective approach to motor control in contrast to alternative VFD methods.

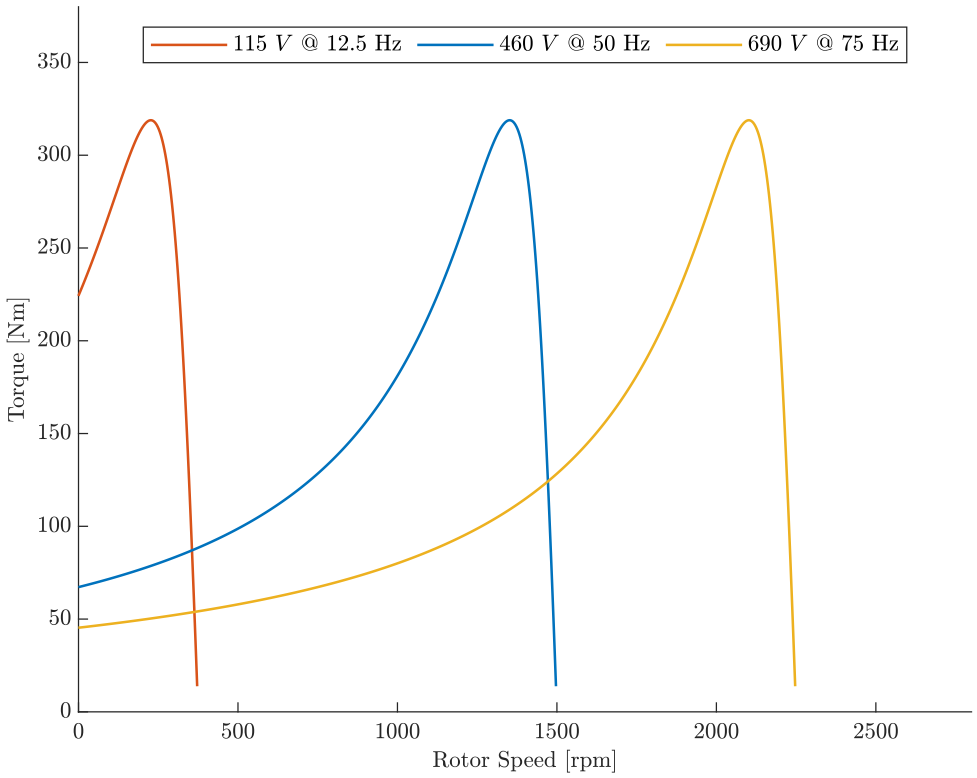


Figure 1.3: Torque-speed curve of an induction motor operated at different voltages with constant U/f ratio.
Source: Created using MATLAB.

The characteristic curve depicted in Figure 1.2 exhibits consistent shape regardless of variations in frequency and voltage that occur in direct proportion. However, the key

distinction lies in the point at which it attains maximum torque, as illustrated in Figure 1.3. This indicates that the curve maintains its overall shape under $^{U}/_{f}$, but undergoes horizontal displacement as the frequency changes [4, p. 472].

Direct Torque Control

Direct Torque Control (DTC) is a more advanced motor control technique that estimates motor torque based on current and voltage measurements. It employs a precise and efficient mathematical algorithm to achieve direct control of the motor's torque. This approach requires only basic motor parameters and measurements, and eliminates the need for a modulator [9, no. 1, p. 16]. However, due to the rapid fluctuations in current resulting from the calculation of the inverter's control signals, this method may introduce noise-related issues. Torque and flux are restricted to specific upper and lower limits, with smaller limits resulting in higher accuracy. By minimizing the discrepancy between desired and estimated torque, DTC maximizes the effectiveness of torque control. This method, also known as hysteresis control, exploits the characteristic phenomenon of hysteresis to improve torque control accuracy [4, p. 644].

DTC's torque response is approximately ten times better than most alternating current (AC) or direct current (DC) drives, making the motor more reliable even in the presence of a rapidly changing mechanical load [9, no. 1, p. 14]. Unlike Pulse Width Modulation (PWM), which typically relies on a constant switching frequency, DTC employs a switching frequency that is determined by the change in torque and stator flux of the motor. This dynamic nature of switching frequency ensures the control of torque and flux to be highly responsive and precise [4, p. 556].

Field Oriented Control

Field Oriented Control (FOC), also known as flux vector control, is a more complicated technique used to regulate the speed and torque of a motor. The method accomplishes its objective by effectively aligning the magnetic fields of the stator and rotor in an orthogonal

manner, thereby maximizing the motor's torque output. Compared to other motor control methods such as scalar control, FOC uses more advanced control algorithms and digital signal processing techniques to calculate the optimal current required to produce the desired magnetic field and torque. This current is then fed to the motor's stator windings using power electronics such as inverters, which enables accurate regulation of the motor's speed and torque, even in situations of varying load conditions. It has been shown that this significantly improve the motor's efficiency and performance compared to conventional control techniques [4, p. 630-632].

1.3 Generator Mode Operation

Regenerative operation, also known as regenerative braking, is a feature that allows an induction motor to operate as a generator. In many wind-electric systems, induction motors are utilized to convert wind energy into electrical energy, which can be transmitted to the power grid. In such applications, the power flow within the system is unidirectional. Induction motors always operate at an asynchronous speed relative to the magnetic field in the rotor. The difference between the speed of the motor's shaft and the rotational speed of the magnetic field is referred to as slip speed. Furthermore, Equation 1.1 depicts how the frequency, f, of the voltage and the number of pole pairs, p, affect the motor's synchronous speed, n_1 [9, no. 7, p. 11].

$$n_1 = \frac{f \cdot 60}{p} \tag{1.1}$$

The induction motor operates with positive slip, denoted s, when the speed of the magnetic field in the stator is greater than the shaft's rotational speed. This can be expressed in percent using Equation 1.2, where the rotor speed, n_2, varies with the mechanical load of the motor. In contrast, the synchronous speed of the rotor remains constant as long as the frequency of the applied voltage is constant. Power flows from the electrical grid to the motor in this mode of operation.

$$s = \frac{n_1 - n_2}{n_1} \cdot 100\% \tag{1.2}$$

Considering an electrical train travelling downhill with induction motors directly connected to its wheels, the motors rotates above synchronous speed due to gravitational forces. As the motors rotate above synchronous speed a counter torque, that opposes the increase in speed, is developed, acting as a brake. However, the braking energy returns as electrical energy via the motor's three phase connection [4, p. 319-320]. Figure 1.4 illustrates the transition from motor to generator, with the intersection of the curve through the y-axis defining the transition point, where the slip is equal to 0.

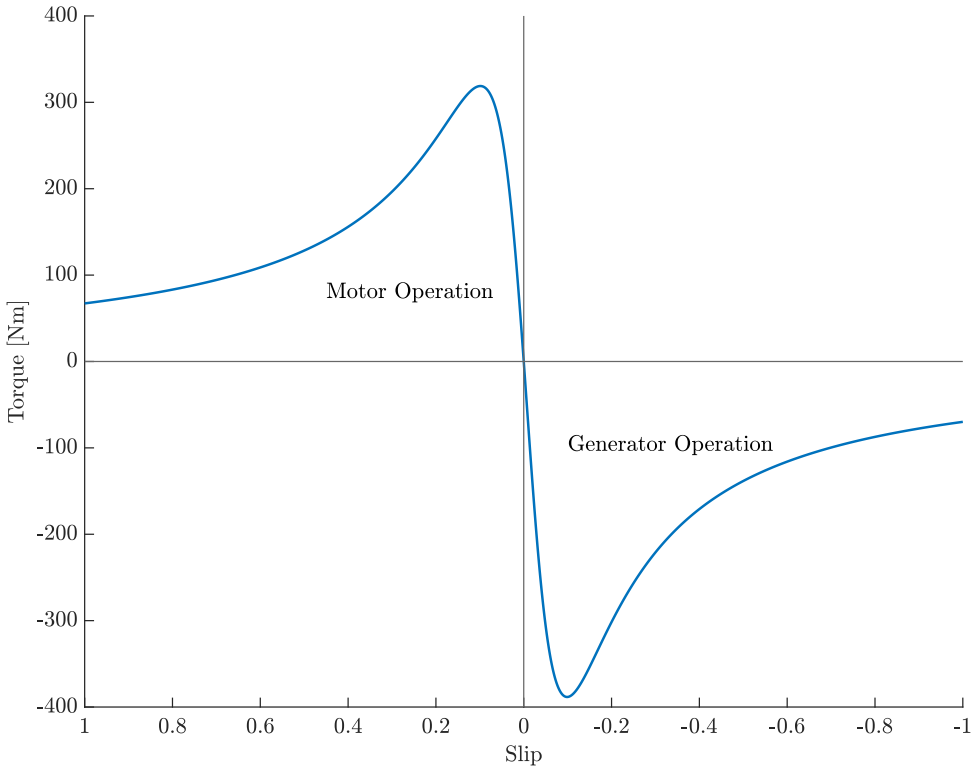


Figure 1.4: Torque-speed curve of an induction motor in motor and generator mode.
Source: Created using MATLAB.

In variable speed drives, the rectifier is usually a 6-pulse or 12-pulse diode rectifier delivering power from the AC grid to the inverter's DC-link. The rectifier can only deliver power unidirectional, allowing power to flow exclusively from the AC grid to the DC-link. If a motor connected to a frequency inverter transitions to regenerative operation, the motor delivers power that charges the DC-link capacitors as shown in Equation 1.3 and 1.4 [9,

no. 2, p. 13].

$$W = P \cdot t = \frac{C \cdot U_{DC}^2}{2} \tag{1.3}$$

$$U_{DC} = \sqrt{\frac{2 \cdot W}{C}} \rightarrow \sqrt{\frac{2 \cdot P \cdot t}{C}} \tag{1.4}$$

Charging of the DC-link capacitors can lead to high voltages that can cause serious damage to the capacitors and the inverter. To prevent excessive voltage increase, there are four primary alternatives available: overvoltage control, braking chopper, Active Front End (AFE), or common DC configuration.

The initial approach entails controlling the power returned from the motor by constraining the braking torque to uphold a consistent DC-link voltage. This method is called overvoltage control, and is a standard feature in most new drives.

The second option for limiting the DC-link voltage is directing the braking energy to a resistor through a braking chopper. The braking chopper is a switch that connects the DC-link to a resistor where the braking energy is dissipated and converted into heat. The braking function is automatically activated when the DC-link voltage exceeds a set limit. This method is a simple circuit design and is inexpensive to implement. A significant disadvantage is that the dissipated energy becomes futile if the heated air cannot be harnessed for any useful purpose.

The third alternative involves employing an inverter with Active Front End capability. This type of inverter incorporates a controlled rectifier, enabling its operation in all four quadrants. Having a bi-directional rectifier allows bi-directional power flow between the AC and DC side of the inverter. This solution is desirable if the motor system generates large braking energy that could be fed back to the AC grid.

In scenarios where a system involves multiple drives, it is possible for one motor to operate in regenerative mode while others continue to function as motors. Consequently, the implementation of a common DC system presents itself as the final option. This system

employs an inverter design that effectively reuses the mechanical energy generated during braking, promoting energy efficiency and resource utilization. The system consists of separate rectifiers and inverters feeding the AC motors, where the common DC bus is the key for moving the braking energy from one motor to benefit the other motors in the system [9, no. 3, p. 15-25].

Chapter 2

Power Conversion with PWM

As previously mentioned, Power Processing Units (PPUs) are integral in adapting the electrical voltage and frequency of the utility line[1], thus enabling the regulation of the rotor speed and torque of the induction machine. As shown in Figure 1, PPUs are composed of two primary constituents. The rectifying section, also known as a rectifier, converts alternating current to direct current, establishing a DC-link. The alternating section, referred to as an inverter, utilizes Pulse Width Modulation (PWM) on the DC-link to generate a sinusoidal voltage. This chapter provides an introduction to inverters and examines some various modulation techniques that can be employed to regulate the induction machine.

2.1 Three-Phase Two-Level Inverters

Inverters are primarily utilized to convert DC to AC, which is useful in mobile applications where only DC power is available. However, due to the underlying technique, inverters are also employed in situations where AC power is already accessible. Figure 2.1 illustrates a three-phase two-level inverter composed of a DC-link and six transistors, two of which form a leg. The transistors operate in pairs as switches that alter the polarity of the

[1] A utility line in electricity refers to the system of wires and equipment that are used to transmit and distribute electrical power from a power plant or substation to customers [13].

voltages U_{Ao}, U_{Bo}, and U_{Co}. By turning the transistors on and off in a specific pattern with high frequency, an AC voltage can be replicated. This is adjustable in terms of amplitude and frequency, subject only to constraints imposed by the DC-link and the modulation algorithm utilized.

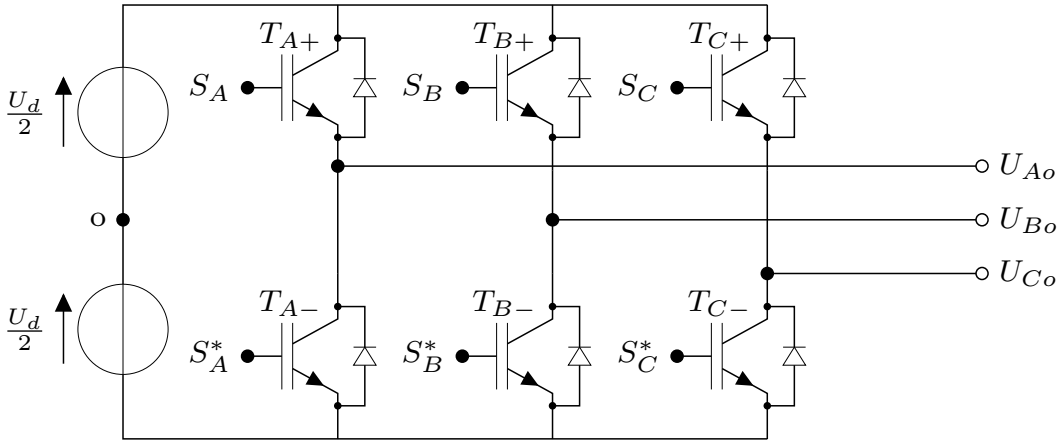


Figure 2.1: Three-phase two-level inverter topology.
Source: Created using CircuiTikZ.

The use of Pulse Width Modulation is ubiquitous in the operation of inverters across various applications. Irrespective of the specific application, the fundamental principle behind PWM remains constant. In essence, the technique involves generating variable-width pulses to mimic the amplitude of an analog input signal. The modulated signal produced in this manner can accurately replicate the desired AC voltage waveform. Although diverse PWM algorithms exist, the underlying principle remains predominantly the same.

Duty Cycle

Pulse Width Modulation entails modulating a square wave signal that alternates between two voltage levels, U_{max} and U_{min}, at high frequencies over a period T_s. The duration of the signal at the high and low levels, referred to as on-time, T_{on}, and off-time, T_{off}, respectively, is determined by a parameter known as the duty cycle, denoted by D, as expressed in Equation 2.1 [3, p. 162].

$$\begin{aligned} D &= \frac{T_{on}}{T_{on} + T_{off}} \\ &= \frac{T_{on}}{T_s} \end{aligned} \tag{2.1}$$

The duty cycle represents the proportion of the signal's period during which it remains in the high state. Mathematically, the relationship between the duty cycle and the average voltage, $\overline{U}$, can be represented as demonstrated in Equation 2.2.

$$\begin{aligned} \overline{U} &= \frac{1}{T_s} \left(\int_0^{D \cdot T_s} U_{max}\, dt + \int_{D \cdot T_s}^{T_s} U_{min}\, dt \right) \\ &= \frac{1}{T_s} \left(D \cdot T_s \cdot U_{max} + (1 - D) \cdot T_s \cdot U_{min} \right) \\ &= D \cdot U_{max} + (1 - D) \cdot U_{min} \end{aligned} \tag{2.2}$$

In the context of inverters, PWM is applied to a DC-link, wherein the voltage have linearity with a nearly steady value. As a result, U_{min} is not applicable, allowing for a further simplification of Equation 2.2:

$$\overline{U} = D \cdot U_{max} \tag{2.3}$$

Figure 2.2 illustrates the correlation between duty cycle and average output voltage, where various duty cycles are represented in relation to a DC-link voltage of 1000 V. The figure consists of five time periods at a switching frequency of 1 kHz, which is introduced in the subsection that follows.

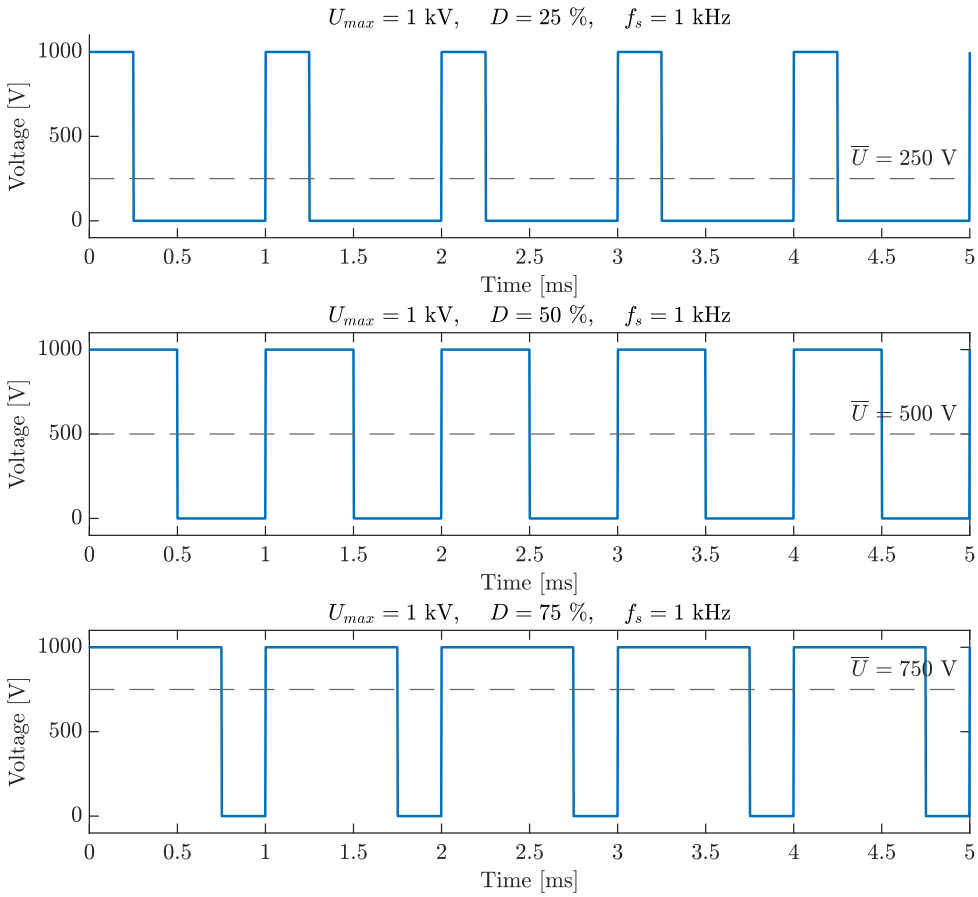


Figure 2.2: Relationship between PWM parameters.
Source: Created using MATLAB.

Switching Frequency

The switching frequency, f_s, refers to the number of times the signal oscillates between the on and off states within the time period T_s [7, p. 48]. This correlation can be expressed using Equation 2.4.

$$f_s = \frac{1}{T_s} \tag{2.4}$$

A higher switching frequency yields greater precision in the generated voltage, however, it is accompanied by increased power losses in practical semiconductor applications. It should also be noted that the switching frequency exerts no influence on the averaged output voltage.

2.2 Sinusoidal Pulse Width Modulation

Sinusoidal Pulse Width Modulation (SPWM) is a widely used modulation technique that generates a sinusoidal voltage waveform through the manipulation of a carrier signal's frequency. When reasonable configured, it is a straightforward and efficacious approach, yielding minimal harmonic distortion. Nevertheless, it has the drawback of not fully utilizating the available DC-link voltage.

Working Principle

The operation of Sinusoidal Pulse Width Modulation involves the comparison between a sinusoidal waveform, denoted as the control signal, $U_{control}$, and a triangular waveform, referred to as the carrier signal, U_{tri}. The frequency of the sinusoidal waveform, f_1, determines the frequency of the output voltage, while the frequency of the triangular waveform determines the switching frequency, f_s, and implies the number of times the transistors change state within a period T_s [3, p. 203].

In an inverter design, the switches T_{X+} and T_{X-} are controlled by comparing the control signal with the carrier signal, resulting in an output voltage, U_{Xo}, that is half the voltage of the DC-link, either positive or negative [3, p. 204]:

$$U_{control} > U_{tri}, \qquad T_{X+} \text{ is on}, \qquad U_{Xo} = \frac{U_d}{2} \tag{2.5a}$$

$$U_{control} < U_{tri}, \qquad T_{X-} \text{ is on}, \qquad U_{Xo} = \frac{-U_d}{2} \tag{2.5b}$$

A comparison of three such control signals and the carrier signal governs the state of the switches at each leg, as shown in Figure 2.3. The conjugation between these prevents the occurrence of a scenario where both switches are in the same state, thus avoiding any possibility of a short circuit in the DC-link.

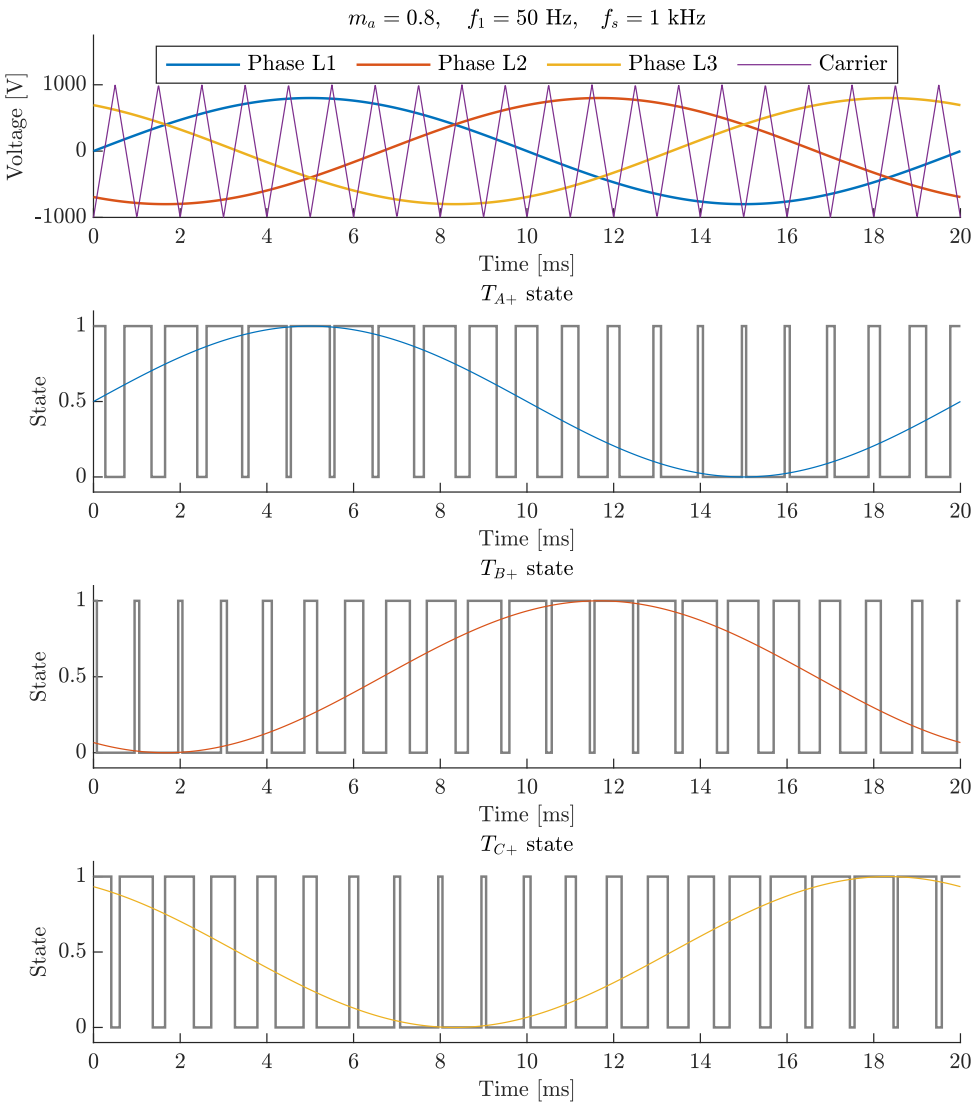


Figure 2.3: Working principle of a three-phased two-level Sinusoidal PWM modulated inverter.
Source: Created using MATLAB.

Linear Modulation

The interplay between the amplitudes of the control signal, $\hat{U}_{control}$, and the carrier signal, $\hat{U}_{tri}$, gives rise to a novel concept known as the amplitude modulation index, m_a, as explicated in Equation 2.6.

$$m_a = \frac{\hat{U}_{control}}{\hat{U}_{tri}} \tag{2.6}$$

Since the maximum value of the carrier signal remains largely constant, the amplitude modulation index is affected only by changing the control signal. An increased amplitude modulation index implies a stronger modulation of the carrier signal's amplitude, which leads to a broader spectrum of output voltages. However, this amplifies the distortion in the output voltage and can have a negative impact on the overall performance.

Assuming a carrier signal with an amplitude greater than or equal to the instantaneous value of the control signal, the average voltage, U_{Xo}, over a switching period can be expressed as the ratio between the two signals and the available DC-link voltage [3, p. 205], as shown in Equation 2.7.

$$U_{Xo} = \frac{U_{control}}{\hat{U}_{tri}} \cdot \frac{U_d}{2}, \qquad U_{control} \leq \hat{U}_{tri} \tag{2.7}$$

Thus, the resultant instantaneous phase voltage of the fundamental frequency component, U_{Xo1}, can be sinusoidally expressed using Equation 2.8, while its peak voltage, $\hat{U}_{Xo1}$, can be derived from Equation 2.9 [3, p. 206].

$$\begin{aligned} U_{Xo1} &= \frac{\hat{U}_{control}}{\hat{U}_{tri}} \cdot \frac{U_d}{2} \cdot \sin\left(\omega_1 \cdot t\right), \qquad && \hat{U}_{tri} \geq \hat{U}_{control} \\ &= m_a \cdot \frac{U_d}{2} \cdot \sin\left(\omega_1 \cdot t\right), && m_a \leq 1.0 \end{aligned} \tag{2.8}$$

$$\hat{U}_{Xo1} = m_a \cdot \frac{U_d}{2}, \qquad m_a \leq 1.0 \tag{2.9}$$

The aforementioned expressions assert that the output RMS line voltage, $U_{LL_{RMS}}$, within the linear region is ascertainable as $\sqrt{3}/\sqrt{2}$ of the phase voltage, $\hat{U}_{Xo1}$, as evinced subsequently in Equation 2.16 within Section 2.3 explicating the Space Vector Pulse Width Modulation technique.

Overmodulation

As explicitly expressed by Equation 2.9, the output voltage exhibits a linear variation with respect to the amplitude modulation index as long as it remains below 1.0. However, if the amplitude of the control signal surpasses that of the carrier signal ($m_a > 1.0$), the inverter enters a region known as the overmodulating region [3, p. 208]. Within this region, the output voltage will contain a larger number of harmonics compared to linear modulation, and it will no longer vary linearly with the amplitude modulation index [3, p. 209].

Describing precisely what happens to the output voltage in the overmodulating region is complex[2], but one of the most influential factors is the frequency modulation index, m_f, defined in Equation 2.10, which, in conjunction with the amplitude modulation index, affects the output voltage of the inverter.

$$m_f = \frac{f_s}{f_1} \tag{2.10}$$

Various sources of literature provide varying perspectives on the overmodulating region. However, the primary reference source for this project recommends the carrier signal and control signal to be synchronized with each other to limit the harmonic content. This is achieved by utilizing values of $m_f \leq 21$ [3, p. 208], which contrasts with the linear region where modulation is largely unaffected by m_f, at least for $m_f > 9$ [3, p. 209].

[2] A methodology for estimating the amplitude modulation index within the nonlinear region is provided herein [2].

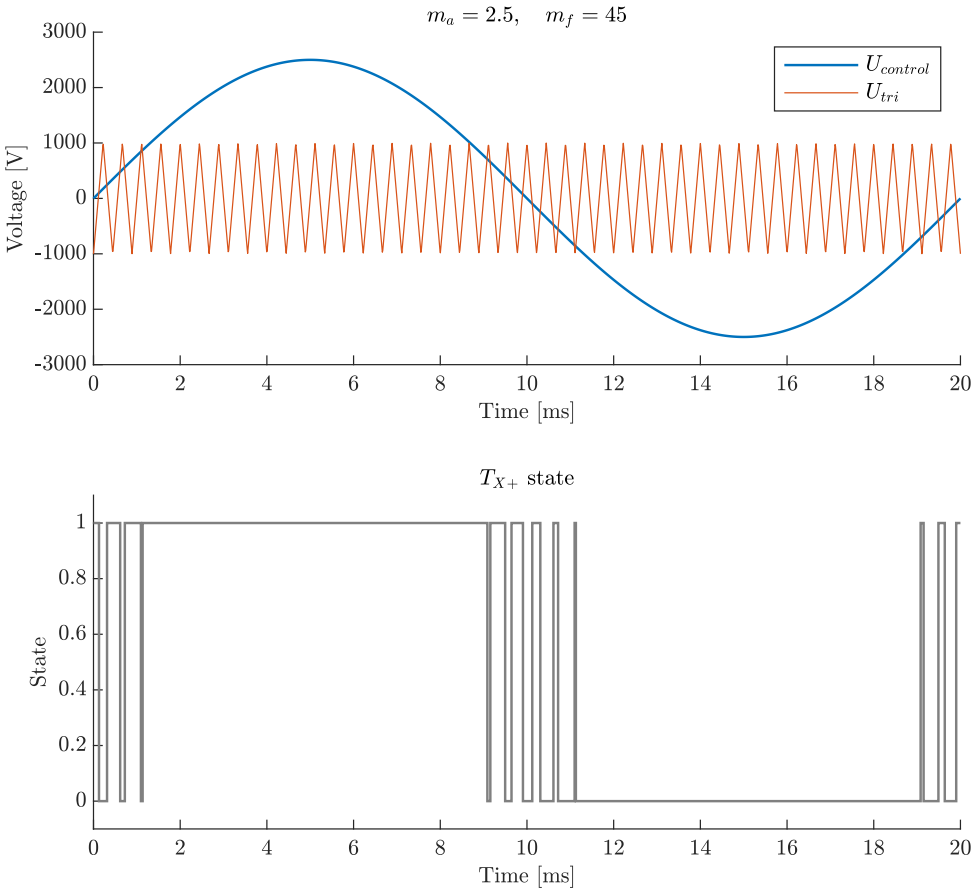


Figure 2.4: Sinusoidal PWM in the overmodulating region.
Source: Created using MATLAB.

Figure 2.4 depicts a graphical representation of a modulating signal at a frequency of 50 Hz, exhibiting an amplitude modulation index of 2.5. Notably, the illustration demarcates the critical region of overmodulation, wherein the amplitude of the control signal exceeds that of the carrier signal. Such a condition results in the transistors remaining in a fixed state for extended periods, thereby generating harmonic frequencies.

Square Wave Operation

When the above is combined with the control signal being of a sufficiently high magnitude compared to the carrier signal ($m_a \gg 1.0$), the output voltage is no longer composed of pulse width modulated transistor switches, and the inverter transitions into square wave operation. In this mode of operation, the output voltage peak is limited to $4/\pi$ of half the DC-link voltage, as expressed by the following equation:

$$\hat{U}_{Xo1} = \frac{4}{\pi} \cdot \frac{U_d}{2}, \qquad m_a \gg 1.0 \tag{2.11}$$

Figure 2.5 is plotted for 3/2 periods of the same modulating signal as in Figure 2.4, illustrating the behavior of the transistor signals as the control signal reaches a level where the carrier signal intersects it solely at the sinusoidal zero-crossing.

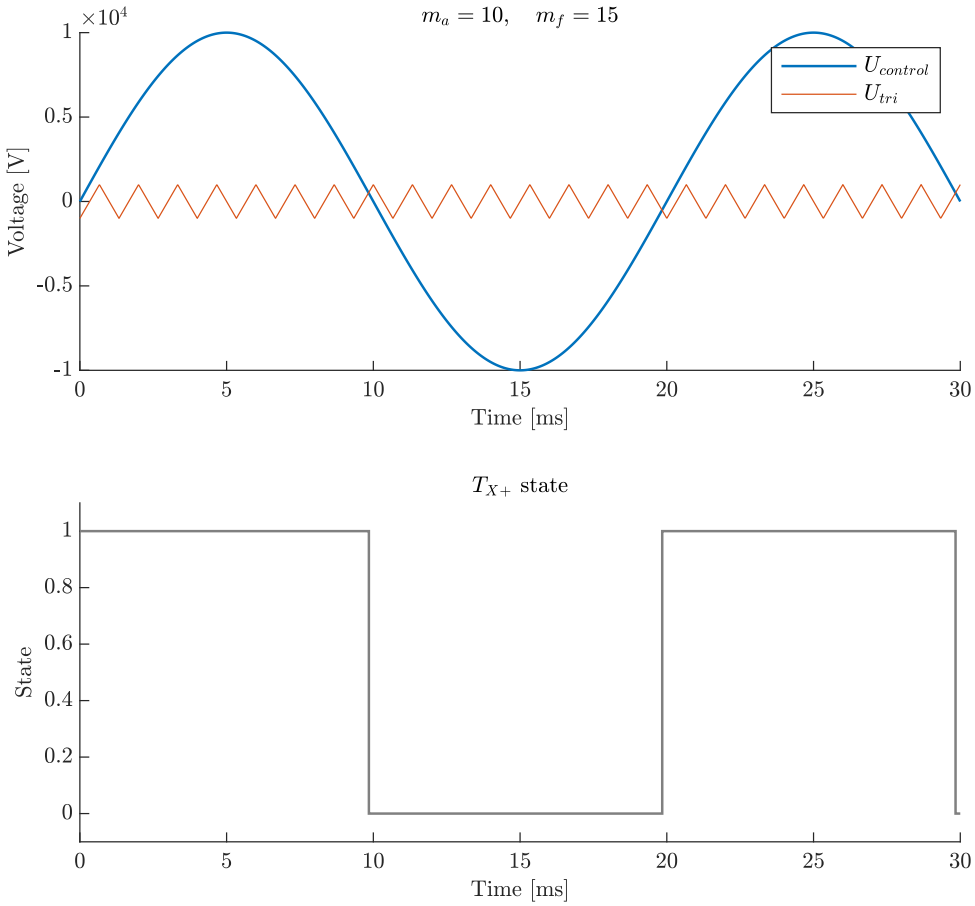


Figure 2.5: Sinusoidal PWM in square wave operation.
Source: Created using MATLAB.

As can be observed from the figure, the transistors are triggered only twice during a period, which is advantageous in high-power applications with slower turn-on and turn-off speeds [3, p. 210], but impractical in a design where control of speed and torque of electric induction motors is desired. This is because of the limitation presented in Equation 2.11, which explicitly states that the output voltage can only be varied with the DC-link voltage.

2.3 Space Vector Pulse Width Modulation

Space Vector Pulse Width Modulation (SV-PWM) is a more advanced modulation technique frequently employed in three-phase inverters. It effectively addresses the drawbacks of conventional Pulse Width Modulation techniques, including the Sinusoidal PWM algorithm, by optimizing the usage of the available DC-link voltage. This modulation technique enables a higher amplitude modulation index relative to SPWM, resulting in an increased output voltage beyond the achievable limits of SPWM.

Working Principle

The Space Vector Pulse Width Modulation technique functions the same way as SPWM by comparing a sinusoidal control signal, $U_{control}$, and a triangular carrier signal, U_{tri}, to determine the states of the individual transistors. The fundamental frequency, f_1, of the output voltage from the inverter is still determined by the control signal's frequency within the period T_s, while the triangular waveform's frequency establishes the switching frequency, f_s.

Although SV-PWM and SPWM share similarities in their basic operating principles, they diverge in the shape of the control signal throughout the period. Specifically, SV-PWM introduces a third harmonic component into the sinusoidal control signal, resulting in a more complex waveform, as depicted in Figure 2.6. The inclusion of such a harmonic component enhances the utilization of the DC-link voltage, U_d, by allowing a higher amplitude modulation index[3], m_a.

[3] $m_a > 1.0$ is still defined as overmodulation.

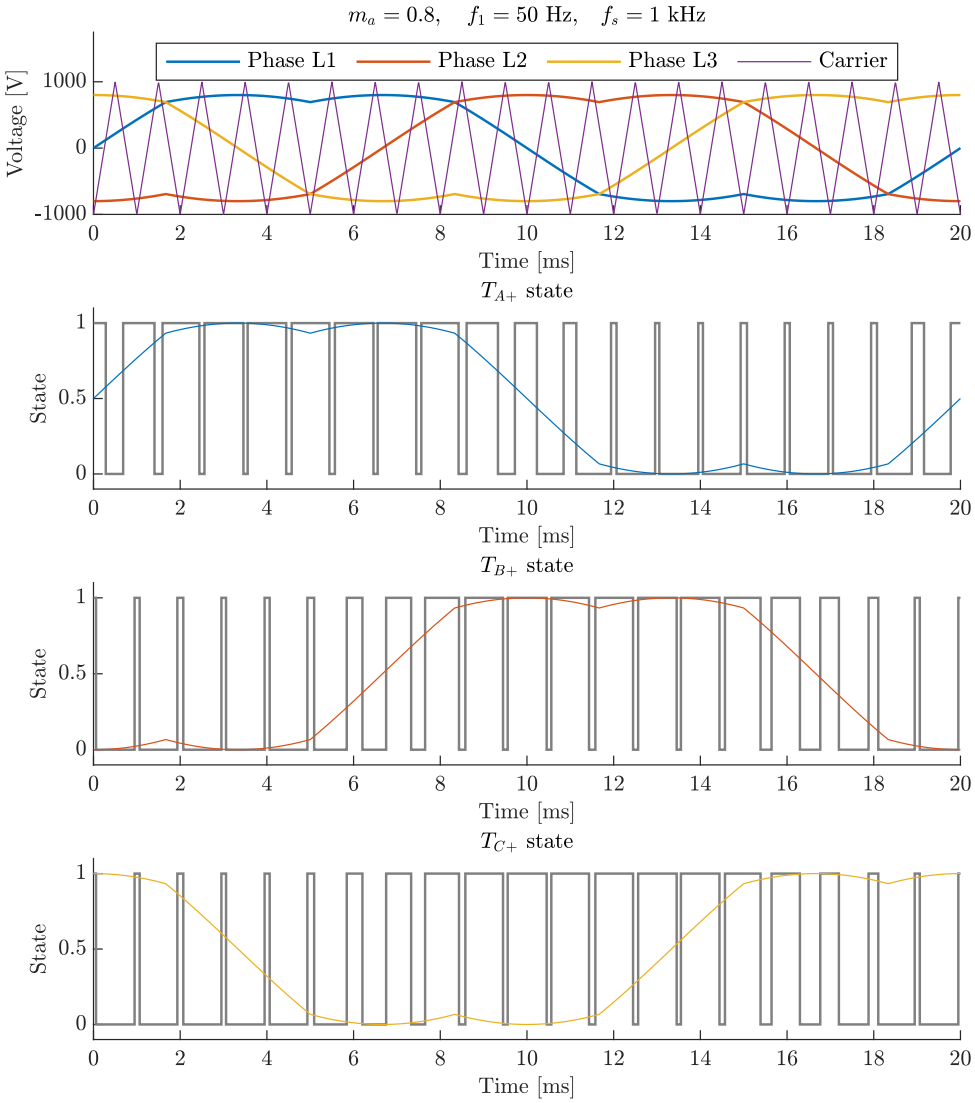


Figure 2.6: Working principle of a two-level Space Vector PWM modulated inverter.
Source: Created using MATLAB.

As can be seen from the figure, the states of the upper and lower transistors, T_{X+} and T_{X-}, are determined based on the same comparison criteria presented in Equation 2.5, where $U_{control} > U_{tri}$ indicates that the upper transistor conducts, whereas $U_{control} < U_{tri}$ implies that the lower one conducts. Similar to the technique of SPWM, there exists no situation where the upper and lower transistors possess an identical state, regardless of the leg. Hence, there are two distinct states for each of the three legs, leading to a total of $2^3 = 8$ possible combinations of the control signals, as illustrated in Table 2.1 [8, p. 121].

Vector	State	Voltage
$\vec{u}_0$	$\vec{u}_s\,(000)$	$0\,\mathrm{V}$
$\vec{u}_1$	$\vec{u}_s\,(001)$	$U_d e^{j0} = U_d \angle 0°$ V
$\vec{u}_2$	$\vec{u}_s\,(010)$	$U_d e^{j\frac{2\pi}{3}} = U_d \angle 120°$ V
$\vec{u}_3$	$\vec{u}_s\,(011)$	$U_d e^{j\frac{\pi}{3}} = U_d \angle 60°$ V
$\vec{u}_4$	$\vec{u}_s\,(100)$	$U_d e^{j\frac{4\pi}{3}} = U_d \angle -120°$ V
$\vec{u}_5$	$\vec{u}_s\,(101)$	$U_d e^{j\frac{5\pi}{3}} = U_d \angle -60°$ V
$\vec{u}_6$	$\vec{u}_s\,(110)$	$U_d e^{j\pi} = U_d \angle 180°$ V
$\vec{u}_7$	$\vec{u}_s\,(111)$	$0\,\mathrm{V}$

Table 2.1: Zero and basic voltage vectors for a two-level inverter.

Each binary digit within the system represents the states of the transistors associated with each leg within the inverter. A binary value of 1 signifies that the upper transistor is conducting, while a binary value of 0 indicates that the lower transistor is conducting. By alternation between these two states, it becomes possible to synthesize an average voltage space vector, as elaborated upon in the subsequent subsections.

Voltage Space Vectors

Unlike SPWM which employs three modulators to generate an equivalent number of phase voltages, SV-PWM utilizes a single modulator known as a reference voltage space vector, represented as $\vec{u}_s$. This vector is the vector sum of the three sinusoidal waveforms known from a conventional three-phase design, with each phase being 120 degrees apart, as shown in Equation 2.12 [8, p. 119]. Consequently, the magnitude of the reference voltage vector typically remains constant regardless of its spatial angle, denoted by θ_s, that determines its location within the time period, T_s.

$$\begin{aligned}\vec{u}_s(t) &= U_{Ao}(t)\, e^{j0} + U_{Bo}(t)\, e^{j\frac{2\pi}{3}} + U_{Co}(t)\, e^{j\frac{4\pi}{3}} \\ &= U_{Ao}(t)\, \angle 0^\circ + U_{Bo}(t)\, \angle 120^\circ + U_{Co}(t)\, \angle -120^\circ\end{aligned} \tag{2.12}$$

The speed at which the vector rotates from 0 to 360 degrees defines the fundamental frequency, f_1, of the three sinusoidal voltages that are generated. Along its path, the vector transverses six distinct sectors, each separated by a 60-degree displacement and bound by their neighboring basic voltage vectors, $\vec{u}_{1-6}$, as depicted in Figure 2.7. It is noteworthy that the two zero vectors, $\vec{u}_0(000)$ and $\vec{u}_7(111)$, are absent from the illustration.

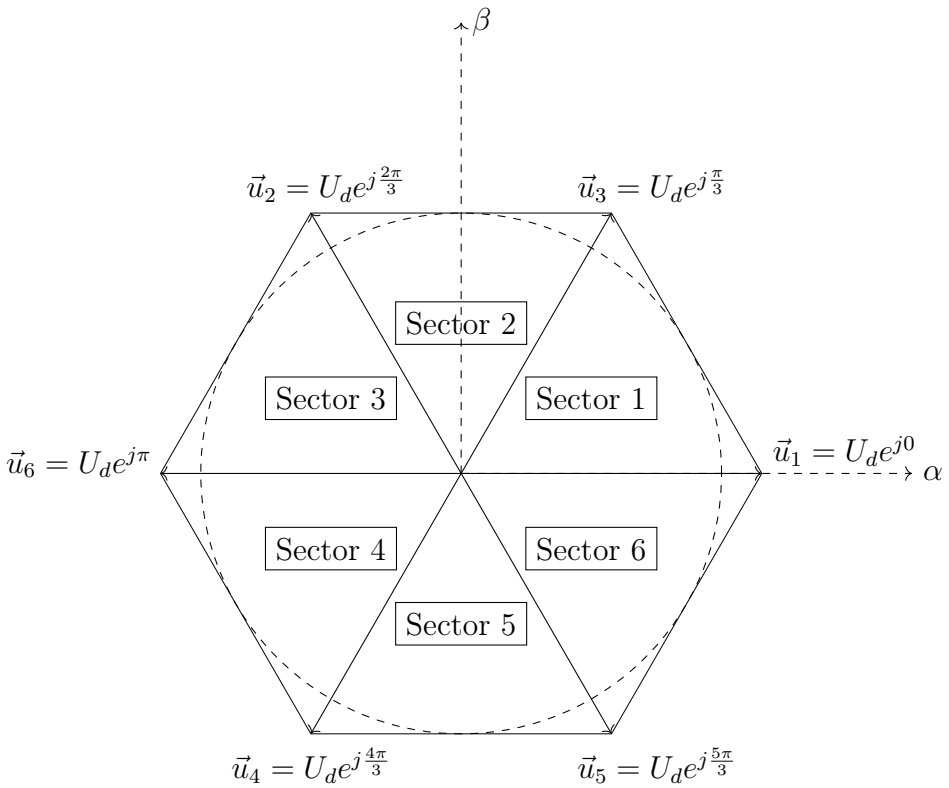


Figure 2.7: Basic voltage vector hexagon (zero vectors not shown).
Source: Created using CircuiTikZ.

Every basic vector denotes the state of a leg with respect to the conductance of the six transistors, or alternatively, the level of voltage being emitted from the DC-link U_d. Notably, a comparison between the positional arrangement of the basic vectors illustrated in Figure 2.7 and their corresponding states as presented in Table 2.1 indicates that the

SV-PWM algorithm attains a heightened level of energy efficiency, especially in terms of switching losses. This is attributed to the fact that each transition necessitates a change in switch state in only one of the legs.

Synthesizing Output Voltage

The average voltage space vector, $\vec{u}_s^a$, can be synthesized over the time interval T_s by computing the durations $\underbrace{xT_s \text{ and } yT_s}_{\alpha \text{ and } \beta \text{ axis}}$, which correspond to the periods during which the two neighboring basic vectors are active. In addition, it is necessary to determine the time period zT_s, during which the two zero vectors are active. For sector 1, shown in Figure 2.8, the average voltage space vector can be expressed using Equation 2.13 [8, p. 122].

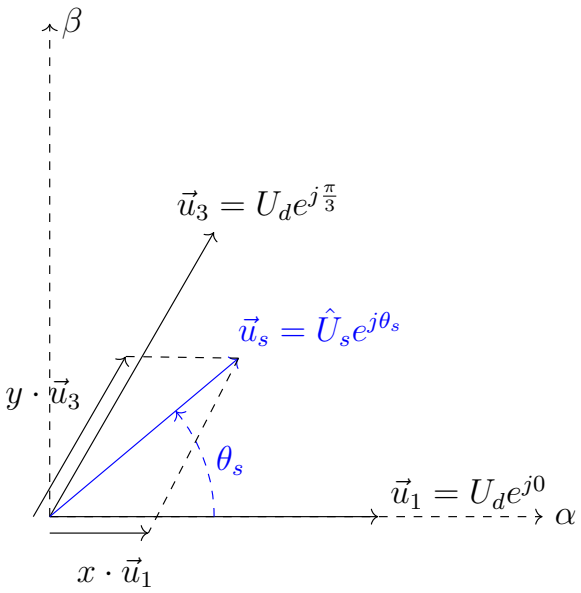


Figure 2.8: Average voltage space vector in sector 1 ($\theta_s = 40°$).
Source: Created using CircuiTikZ.

$$\begin{aligned} \vec{u}_s^a &= \frac{1}{T_s}\left(xT_s \cdot \vec{u}_1 + yT_s \cdot \vec{u}_3 + zT_s \cdot 0\right), \qquad x + y + z = 1 \\ &= x \cdot \vec{u}_1 + y \cdot \vec{u}_3 \end{aligned} \tag{2.13}$$

Table 2.2 facilitates the derivation of Equation 2.13, as well as corresponding equations for the remaining five sectors, by means of the basic vector's amplitude, $\hat{U}_s$, and phase angle, θ_s, relative to the alpha and beta axes, and the DC-link voltage [8, p. 123].

Sector	Equation
1	$\hat{U}_s e^{j\theta_s} = x \cdot U_d e^{j0} + y \cdot U_d e^{j\frac{\pi}{3}}$
2	$\hat{U}_s e^{j\theta_s} = x \cdot U_d e^{j\frac{\pi}{3}} + y \cdot U_d e^{j\frac{2\pi}{3}}$
3	$\hat{U}_s e^{j\theta_s} = x \cdot U_d e^{j\frac{2\pi}{3}} + y \cdot U_d e^{j\pi}$
4	$\hat{U}_s e^{j\theta_s} = x \cdot U_d e^{j\pi} + y \cdot U_d e^{j\frac{4\pi}{3}}$
5	$\hat{U}_s e^{j\theta_s} = x \cdot U_d e^{j\frac{4\pi}{3}} + y \cdot U_d e^{j\frac{5\pi}{3}}$
6	$\hat{U}_s e^{j\theta_s} = x \cdot U_d e^{j\frac{5\pi}{3}} + y \cdot U_d e^{j0}$

Table 2.2: Average voltage space vector equations.

The equations presented in Table 2.2 are composed of a real component and an imaginary component. Utilizing Euler's formula[4], these components can be expressed as products of cosine and sine functions, which can be further decomposed into their respective $\underbrace{\text{real and imaginary}}_{\Re \text{ and } \Im}$ constituents. This implies that the duration at the α and β coordinates in each sector can be modeled by separate expressions, as elucidated in Table 2.3.

Sector	$\Re(\hat{U}_s e^{j\theta_s})$	$\Im(\hat{U}_s e^{j\theta_s})$
1	$\hat{U}_s \cos\theta_s = x \cdot U_d + y \cdot U_d \cdot \frac{1}{2}$	$\hat{U}_s \sin\theta_s = y \cdot U_d \cdot \frac{\sqrt{3}}{2}$
2	$\hat{U}_s \cos\theta_s = x \cdot U_d \cdot \frac{1}{2} - y \cdot U_d \cdot \frac{1}{2}$	$\hat{U}_s \sin\theta_s = x \cdot U_d \cdot \frac{\sqrt{3}}{2} + y \cdot U_d \cdot \frac{\sqrt{3}}{2}$
3	$\hat{U}_s \cos\theta_s = -x \cdot U_d \cdot \frac{1}{2} - y \cdot U_d$	$\hat{U}_s \sin\theta_s = x \cdot U_d \cdot \frac{\sqrt{3}}{2}$
4	$\hat{U}_s \cos\theta_s = -x \cdot U_d - y \cdot U_d \cdot \frac{1}{2}$	$\hat{U}_s \sin\theta_s = -y \cdot U_d \cdot \frac{\sqrt{3}}{2}$
5	$\hat{U}_s \cos\theta_s = -x \cdot U_d \cdot \frac{1}{2} + y \cdot U_d \cdot \frac{1}{2}$	$\hat{U}_s \sin\theta_s = -x \cdot U_d \cdot \frac{\sqrt{3}}{2} - y \cdot U_d \cdot \frac{\sqrt{3}}{2}$
6	$\hat{U}_s \cos\theta_s = x \cdot U_d \cdot \frac{1}{2} + y \cdot U_d$	$\hat{U}_s \sin\theta_s = -x \cdot U_d \cdot \frac{\sqrt{3}}{2}$

Table 2.3: Real and imaginary parts of the average voltage space vector equations.

[4] Euler's formula: $e^{j\theta_s} = \cos\theta_s + j\sin\theta_s$.

Through the utilization of the relationships delineated in Table 2.3, it becomes feasible to synthesize the desired average voltage space vector in a two-level inverter, independent of its sectorial position.

Linear Modulation

Within its linear modulation range ($m_a \leq 1.0$), SV-PWM leverages the available DC-link voltage more efficiently, owing to its inherent characteristic of third harmonic injection. The magnitude of the generated voltages is contingent upon the maximum amplitude of the average voltage vector, which is constrained by the boundary of the circle enclosed within the hexagonal region depicted in Figure 2.7. As these boundaries serves as a representation of the DC-link voltage, the maximum output voltage that can be generated is situated at the midpoint between two basic vectors, where θ_s equals $^{60}/_{2}$ degrees. In this regard, the voltage amplitude can be mathematically expressed through a cosine function, as shown in Equation 2.14 [8, p. 125].

$$\begin{aligned} \hat{U}_{s,max} &= U_d \cdot \cos 30^\circ \\ &= \frac{\sqrt{3}}{2} \cdot U_d \end{aligned} \tag{2.14}$$

Furthermore, this implies that the peak voltage of the fundamental frequency component, $\hat{U}_{Xo1}$, can be expressed as a function of the amplitude modulation index, as shown in Equation 2.15, similar to Equation 2.9 for SPWM [8, p. 128].

$$\hat{U}_{Xo1} = m_a \cdot \frac{U_d}{\sqrt{3}}, \qquad m_a \leq 1.0 \tag{2.15}$$

Upon comparing Equation 2.9 with the aforementioned equations, it becomes apparent that SV-PWM, assuming identical conditions ($m_a \leq 1.0$), can synthesize an output RMS line voltage, $U_{LL_{RMS}}$, that is $^{2}/_{\sqrt{3}}$, or approximately 15 %, higher than what is attainable

with SPWM, as shown in Equations 2.16 and 2.17. This advantage is attributable to the injection of the third harmonic component in the control signals of the SV-PWM algorithm.

$$\begin{aligned} \text{SPWM:} \qquad U_{LL_{RMS}} &= \sqrt{3} \cdot \frac{\overbrace{\hat{U}_{Xo1}}^{\text{Eq. 2.9}}}{\sqrt{2}} \\ &= \underbrace{m_a \cdot \frac{\sqrt{3} \cdot U_d}{2\sqrt{2}}}_{\approx m_a \cdot 0.612 \cdot U_d}, \qquad m_a \leq 1.0 \end{aligned} \tag{2.16}$$

$$\begin{aligned} \text{SV-PWM:} \qquad U_{LL_{RMS}} &= \sqrt{3} \cdot \frac{\overbrace{\hat{U}_{Xo1}}^{\text{Eq. 2.15}}}{\sqrt{2}} \\ &= \underbrace{m_a \cdot \frac{U_d}{\sqrt{2}}}_{\approx m_a \cdot 0.707 \cdot U_d}, \qquad m_a \leq 1.0 \end{aligned} \tag{2.17}$$

Non-Linear Modulation

Similar to the behavior observed in the case of SPWM, the output voltage generated from the SV-PWM technique exhibits an increased level of harmonic distortion as the control signal exceeds the amplitude of the carrier signal ($m_a > 1.0$). Figure 2.9, generated under identical experimental conditions as Figure 2.4 for SPWM, presents an illustrative representation of the transistor signals within this operating region.

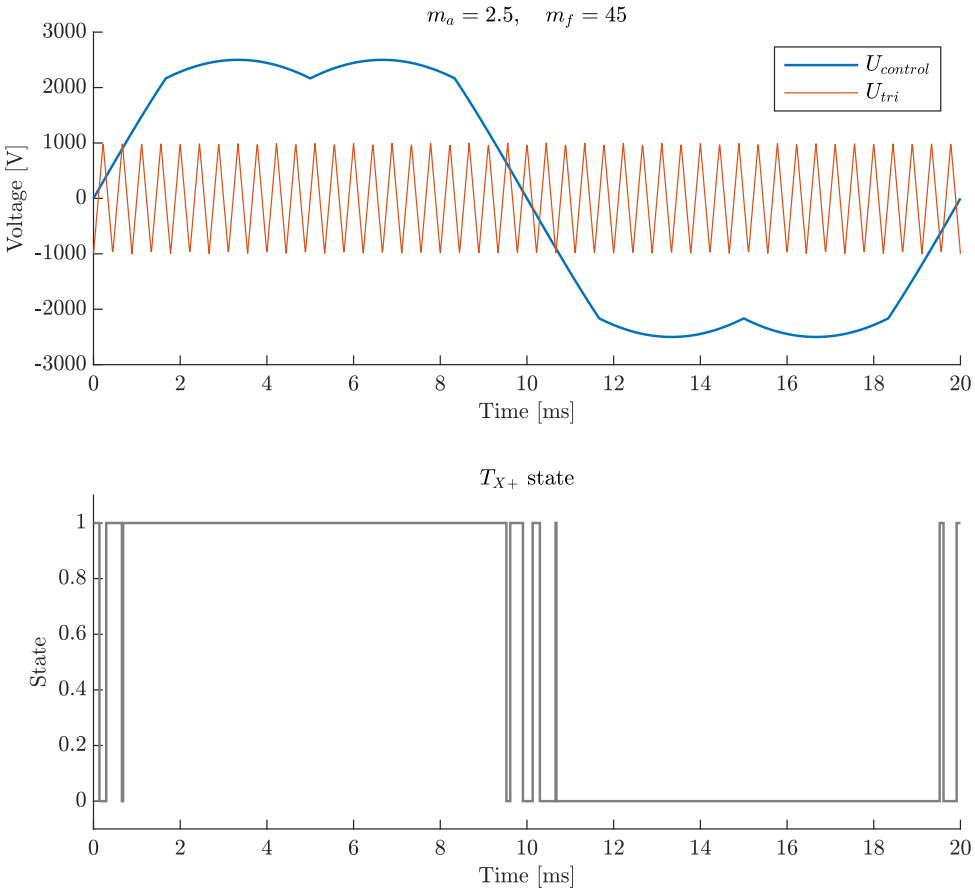


Figure 2.9: Space Vector PWM in the overmodulating region.
Source: Created using MATLAB.

By increasing the amplitude modulation index to a considerably elevated value ($m_a \gg 1.0$), the inverter undergoes a transition to square wave operation, as exemplified in Figure 2.5 for SPWM. Determining the precise value of m_a required to trigger this transition is a complicated matter[5]. However, the ratio between m_a and m_f has a significant impact as it determines the point at which the control signal and carrier signal intersect.

[5] A valuable resource for scrutinizing the behavior of the output voltage within the nonlinear region is the original research article on Space Vector Pulse Width Modulation, which is referenced herein [1].

Part II

Development

Chapter 3

Demands and Specifications

This chapter has been formulated in conjunction with the employer and the supervisor with the aim of ensuring a comprehensive and unambiguous definition of the scope of this project. The chapter is structured into two distinct sections, the first of which outlines the requirements for implementation and the second specifying standards for documenting them.

3.1 Design Requirements

In general, an electric device is to be fabricated converting DC to three-phase AC. The specific requirements for execution are specified in the subsections that follows.

Electrical Specifications

To execute the conversion effectively, the modulation technique of choice shall be SV-PWM, and the control signals should be generated using a 32-bit STM microcontroller. Furthermore, the electrical specifications of the inverter must comply with the parameters outlined in Table 3.1.

Parameter	Nominal	Peak
DC-link Voltage	565 V_{DC}	1000 V_{DC}
Output Line Voltage	400 V_{RMS}	*ND*
Output Current	5 A_{RMS}	*ND*
Modulation Frequency	50 Hz	100 Hz
Switching Frequency	$\geq$ 4 kHz	*ND*

Table 3.1: Electrical specifications for the inverter.

Measurements

The completed design also entails specific requirements for circuit measurements. The following measurements must be implemented and calibrated to the ADC on the microcontroller:

- Current through the DC-link
- Voltage across the DC-link
- Both mean and RMS current through all three phases in the output

Protection

To maintain the safety of both personnel and equipment, certain protective measures must be put into place:

- Galvanic isolation between the microcontroller and the power section of the inverter
- Protection from overheating the transistors
- Internal short circuit protection
- Protection from electrical shock

3.2 Documentation

In addition to developing a laboratory exercise for future electrical engineering students, the following elements shall be used as documentation for the inverter:

- Circuit diagrams
- Program code
- Simulation results

Chapter 4

Problem Analysis

For the purpose of providing a overview of the demands and specifications set forth by the employer in Chapter 3, the present analysis endeavors to deconstruct the requisite elements that are indispensable for their fulfillment. The primary objective of this segment is to delineate the pertinent factors that necessitate due consideration to accomplish the project. The chapter serves as a foundational framework and has also been utilized to formulate a proposed solution, as demonstrated in Section 4.4.

4.1 Components Selection

The choice of hardware is arguably the most vital aspect for a functional design. This section presents an evaluation of the key factors to keep in mind when selecting the components to be utilized.

Power Supply

A power requirement analysis for all components on the circuit board is imperative in determining the size of the primary power supply. Furthermore, an appropriate voltage level must be established for the most power-intensive components. It is also necessary to

select suitable power supplies for any portion of the circuit that may not exhibit the same voltage level as the primary power supply. The following considerations should inform these determinations:

- Total power required
- Input and output voltage

Additionally, it is necessary to take into account the requirements for galvanic isolation between the microcontroller and the power section of the inverter.

Microcontroller

As per the specifications outlined in Chapter 3.1, it is stipulated that a 32-bit STM microcontroller should be employed. The specific microcontroller that is selected is contingent upon a multitude of factors. Thus, it is imperative to take these into consideration in the evaluation process:

- Minimum six PWM outputs
- One analog input per current and voltage sensor
- Built-in timers supporting advanced motor control
- Sufficient amount of I/O for expansion

Transistors

When confronted with the task of selecting the appropriate type of transistors, there exist three fundamental factors that must be taken into consideration:

- Switching frequency
- Current through the semiconductor
- Voltage across the semiconductor

Gate Drivers

It is necessary to evaluate the potential of utilizing gate drivers as intermediaries between the microcontroller and the gate inputs of the transistors. This may offer advantages such as providing the correct current and voltage at the inputs, thus ensuring ideal operating conditions for the transistors while at the same time protecting the microcontroller from current overload. The selection of gate drivers must be based on the type of transistors.

Temperature Control

In order to adequately address the cooling requirement of the transistors, a suitable cooling solution must be implemented. Both passive and active cooling are potential candidates, and the final choice should be made based on considerations of doability and efficiency. The chosen solution must also be dimensioned in accordance with the anticipated surface temperature during the switching process of the transistors.

Braking Circuit

Chapter 1.3 highlights the necessity of implementing an appropriate system for managing the electrical power produced during regenerative motor operations. The design of such a mechanism is contingent upon the expected magnitude of the power generated.

Current and Voltage Sensors

When considering Chapter 3.1 of the requirement specification with regards to current and voltage measurements, it is crucial to take into account two fundamental elements during the sensor selection process:

- Suitable range
- AC/DC

Other

It is generally advisable to consider the use of surface-mounted components rather than through-hole components as they can contribute to better utilization of circuit board area and make development easier. Factors such as cost and availability also play a crucial role in the decisions that need to be made.

4.2 Software Tools

Conducting such a project necessitates access to data tools with specialized functionality:

- Schematic editor
- PCB editor
- Circuit simulator
- Microcontroller IDE
- Project management tool

4.3 Laboratory Equipment

In order to make it possible to perform tests on prototypes, access to certain electronic equipment is imperative. This section discusses the equipment that is deemed relevant for this purpose.

Rectifier

A rectifier, as shown in Figure 1, is essential for supplying DC voltage to the DC-link of the inverter. As per Table 3.1 of the requirements specification, it should be capable of delivering a minimum of $1000\,\mathrm{V_{DC}}$.

Load Resistor

To conduct tests of the inverter's performance under a purely resistive load, it is necessary to incorporate a suitable load resistor. Given that a three-phase AC voltage is generated, the resistive load must also be configured as a three-phase system. It is imperative that the resistance of the load are sufficiently low to elicit a discernible response from the inverter.

Induction Motor

The induction motor assumes a crucial role in the testing process by enabling an examination of the inverter's performance when subjected to an inductive load. Moreover, it allows for the evaluation of the inverter's speed and torque regulation capabilities, thereby playing an integral part in assessing its motor control functionality. The specification outlined in Table 3.1 requires the inverter to deliver $5\,\mathrm{A_{RMS}}$ at line voltages of $400\,\mathrm{V_{RMS}}$, which implies that the motor should have the capability of matching those nominal specifications.

Measuring Equipment

In order to verify the proper functioning of the microcontroller program, an oscilloscope can serve as proof. It must be capable of handling the outlined current and voltage demands in Table 3.1, as well as frequencies greater or equal to $4\,\mathrm{kHz}$.

Additionally, complementary equipment such as differential probes, current probes, multimeters, and similar are also indispensable. A thermal imaging camera is likewise a mandatory requirement to ascertain that the surface temperature of the circuit board and its components remains within reasonable thresholds.

4.4 Proposed Solution

Based on the preceding discussion, a proposed solution that meets the requirements of the specification has been developed in Figure 4.1. It is worth noting that this has been subject to revision throughout the course of the project, and as such, served merely as a preliminary blueprint from which to work towards a final solution.

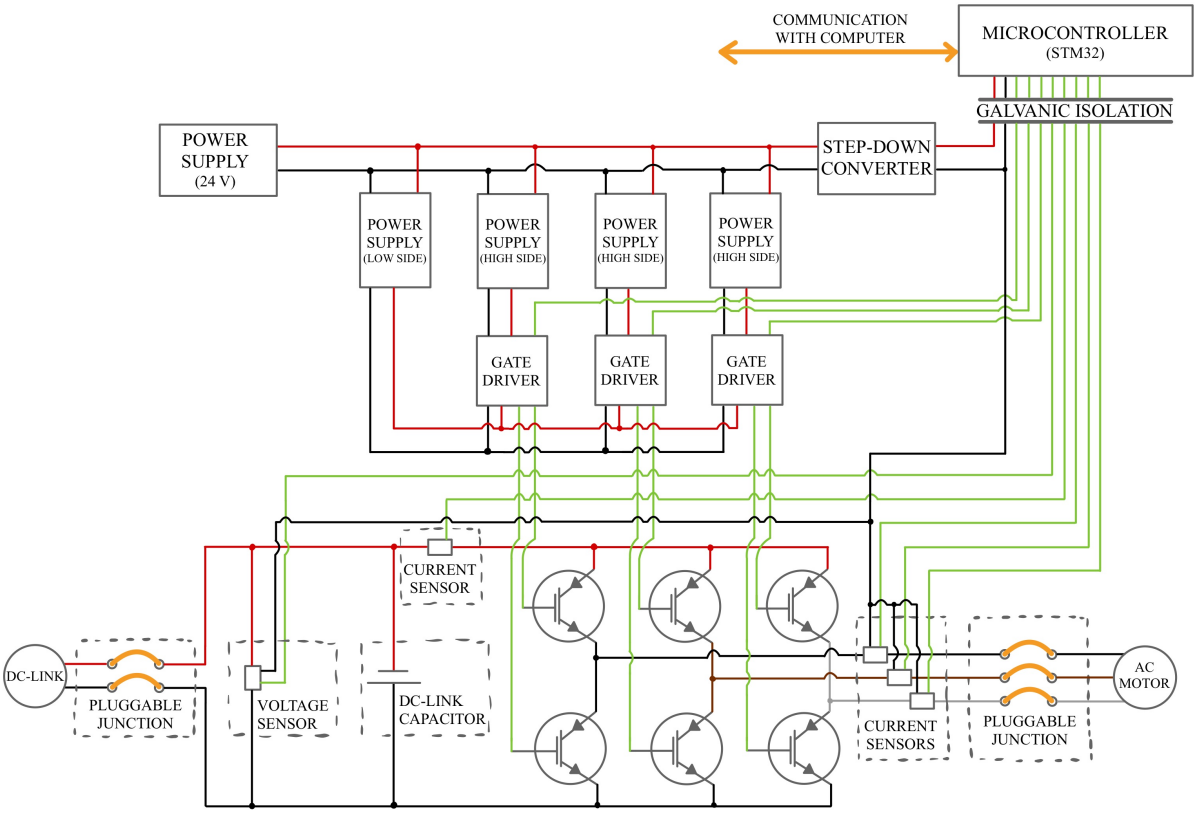


Figure 4.1: Simplified circuit diagram.
Source: Created using GoodNotes.

Chapter 5

Circuit Board Design

In order to achieve operational functionality of the inverter, the utilization of a Printed Circuit Board (PCB) is deemed essential to effectively interconnect all components and their respective sub-circuits. This encompasses the establishment of interconnections among diverse elements such as power supplies, transistors, and the microcontroller. This chapter emphasises essential design considerations, circuit topology, component selection, layout and routing. Furthermore, the chapter addresses the challenges encountered during the design process while presenting practical solutions to overcome them.

5.1 Power Supply Selection

During the development process of the PCB, it became apparent that the provision of multiple voltage levels and power supplies is a necessary and advantageous feature, as expounded in Chapter 4.1. This is due to the requirement for different voltage supplies by diverse chips and circuits, as well as the need for particular power supplies for certain components, such as isolated DC-DC converters. To identify the essential voltage levels to be included on the board, an assessment of the requirements of the various components chosen for the board, was conducted. Furthermore, the voltage levels for the components were determined based on power dissipation and current draw, where feasible. The voltage levels made available on the board are illustrated in the circuit diagrams in Appendix B.

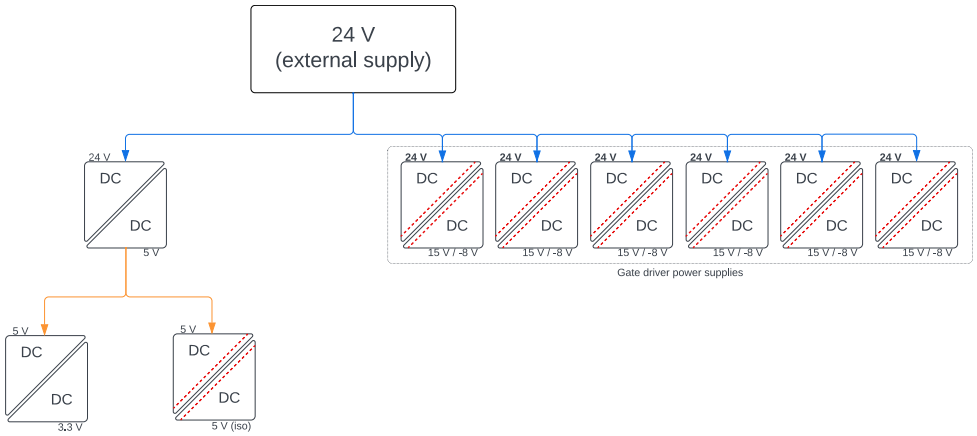


Figure 5.1: Power supply topology.
Source: Created using Lucidchart.

Figure 5.1 illustrates a topological diagram for the power supplies implemented on the PCB. The diagram is a representation of how the components are connected. Furthermore, Table 5.1 provides an overview of the power supply requirements for the different components on the board and serves at the basis for the implemented power supplies.

Voltage	Load	Remark
3.3 V	Microcontroller	Onboard logic
	Microcontroller	I/O signals
	Current sensors	
	Level shifters	5 V to 3.3 V
	I/O expansion card	
5 V	Power supply	Microcontroller
	Level shifters	3.3 V to 5 V
	Gate drivers	Input side
	DC-DC converter	5 V to 3.3 V
	DC-DC converter	5 V to 5 V isolated
	Isolation amplifier	Input side
	Operational amplifiers	
	Comparator	Braking circuit
	LCD display	
5 V isolated	Isolation amplifier	Output side
5 V	DC-DC converter	24 V to 15 V/−8 V
	DC-DC converter	24 V to 5 V
15 V/−8 V	Gate drivers	Output side

Table 5.1: Available voltage levels on the PCB.

To power the 3.3 V components and chips, it was determined to use *Infineon TLS205B0EJV33*. The component was chosen due to its wide input range, up to 20 V, and 500 mA current capability. The chip is equipped with protection mechanisms for both overcurrent and overtemperature. Additionally, it features an output voltage regulator to ensure optimized regulation performance with minimal voltage drops.

To power the 5 V components and chips, it was determined to use *Multicomp Pro MP-K7805T-500R3.* Costs, SMD (Surface Mount Device) package, output short-circuit protection and 500 mA output current made the product a good choice for the design. To supply

5 V isolated power to the voltage measurement circuit as presented in Appendix B.11, the *Murata NTE0505MC* was selected. This product met the design requirements with respect to cost, SMD package and 1 watt output power.

As galvanic isolation had to be implemented in the design, described in detail in Section 5.2, it was necessary to implement isolated DC-DC converters to supply the input side of the gate drivers. *Murata Power Solutions MGJ2D241509SC* was the product of choice. To minimize the current draw from the six power supplies needed in the circuit, it was reasonable to select the 24 V version.

The 24 V power supply is decided to be external. In the test phase, a bench top power supply is desirable to use due to overcurrent detection and short circuit detection. A *Wago 2604-3104* PCB terminal block is implemented to ensure a safe and hassle-free external connection.

5.2 Design of Subcircuits

To interconnect all the systems in the inverter, and meet the demands and specifications in Chapter 3, it is imperative to design a range of electrical circuits. The circuits have been developed in accordance with the design specifications provided by the component suppliers, and have been simulated and constructed under the guidance of the supervisor. The following circuits must be designed based on the fundamental functionalities explicated in Chapter 4.

Transistors

IGBTs (Insulated-Gate Bipolar Transistors) were chosen over other transistor types such as MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) and BJTs (Bipolar Junction Transistors) for their specific characteristics. IGBTs combine the high input impedance of a MOSFET with the low saturation voltage of a BJT, making them very suitable for high power applications. The IGBT has a fast switching speed, which is

necessary for high-frequency switching applications. Their low conduction losses make them highly efficient. IGBTs were the ideal choice for the specific application due to their superior performance characteristics. In the design, *Infineon IKW40N120H3* were chosen due to advantages such as a maximum collector-emitter voltage of 1200 V, collector current of 40 A, low electromagnetic interference (EMI), an integrated anti-parallel diode and TO-247 package.

Controlling Transistors

To establish an interface for controlling and monitoring the switching elements in the circuit, specifically the IGBTs, gate drivers are commonly utilized. Gate drivers act as the intermediary between the microcontroller and the IGBTs, providing a means of communication and control. In this context, the *Infineon 2ED020I12-F2* gate driver was chosen due to its ability to control both IGBTs within a single leg of the inverter, utilizing a single chip. The gate driver supports 600 V/1200 V IGBT applications and possesses V_{CE} saturation detection and active miller clamp features. Moreover, the driver is equipped with pins that connect to the microcontroller, allowing for fault detection and operational status indications.

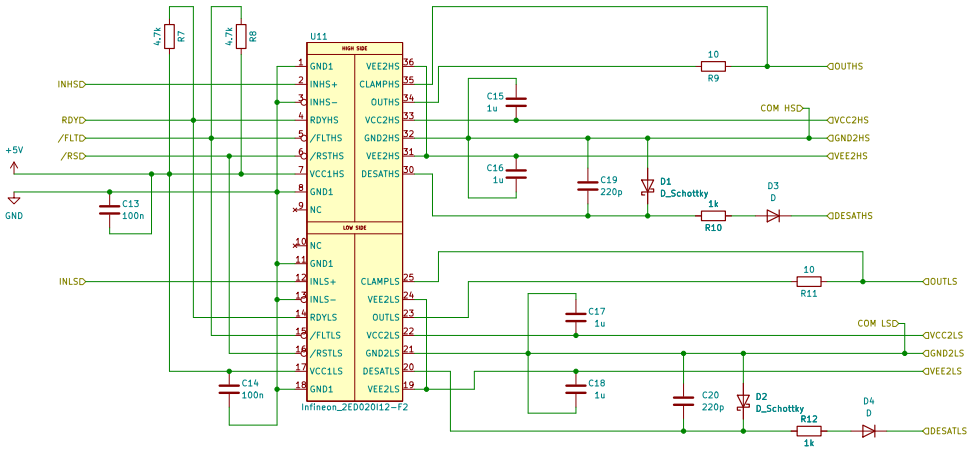


Figure 5.2: Gate driver topology.
Source: Created using KiCad.

Current Measurements

In accordance with Chapter 3 of the inverters requirements, current measurement is to be established in both the DC-link main current and the three outgoing phases. Tu fulfill this requirement, the current sensor *Infineon Technologies TLI4971A050T5UE0001XUMA1* was selected. This component offers a measurement range up to +/- 50 A, 3.3 V power supply, and an analog output to the ACD in the microcontroller. Furthermore, the sensor features two Overcurrent Detection (OCD) outputs, OCD1 and OCD2. These outputs provide capabilities that can be utilized by the microcontroller to establish a safety feature that disables the inverter in the event of excessive current draw.

The resistors and capacitors utilized in the sensor's topology were designed in accordance with the specifications outlined in its datasheet. As illustrated in the circuit diagram in Appendix B.10, a dedicated circuit was designed to establish a reference voltage for the current sensors. This is critical as it is essential to measure both positive and negative currents, which flows in both directions. The microcontroller's ADC (Analog-to-Digital Converter) possesses a measurement range from 0 V-3.3 V. To provide the current sensors with 1.65 V at the V_{REF} pin, resistor R_{25} and R_{26} form a voltage divider. In the absence of current flow through the current sensor, the A_{OUT} pin has a voltage of $V_{REF} = 1.65\,\text{V}$. Any increase or decrease in voltage level at the current sensor's analog output is scaled in accordance with the manufacturer's datasheet, with an increase or decrease in millivolts per ampere passing through the sensor.

Voltage Measurements

According to specifications in Chapter 3, it is needed to measure the DC-link voltage. In nominal operation, the DC-link voltage is intended to be 565 V DC. This voltage needs to be converted to a range that works with the selected microcontroller ADC, to be able to measure the voltage

To realize this setup it is desirable to design a voltage divider, and to build galvanic isolation between the high DC-voltage, and the scaled signal. Implementing *Broadcom*

ACPL-C87B-000E in the design is a prudent approach to accomplish effective galvanic isolation. This chip needs 5 V on both sides. Therefore it was necessary to implement a isolated DC-DC converter (5 V to 5 V isolated) for the purpose. Furthermore, it was deemed important to incorporate an operational amplifier in order to attain the precise input voltage requisite for the analog to digital converter within the microcontroller. Detailed schematics are found in Appendix B.11 for the voltage measurement circuit.

Voltage Divider Design

To ensure proper functionality of the voltage divider, several design considerations must be taken into account. Firstly, the current flowing through the voltage divider should not be too high in order to avoid excessive heat generation and power dissipation in the resistors. Additionally the divider must be designed to measure a voltage of 565 V DC, with sufficient margin for transients, causing the maximum measurable voltage to be limited to 1000 V DC. The resistor being measured over should be selected such that a 0 V to 1000 V DC-link voltage corresponds to a 0 V to 2 V voltage drop across the resistor. Furthermore, the 0 V to 2 V signal fed through the isolated amplifier chip must be properly scaled to fully utilize the measurement range of the ADC in the microcontroller, with a maximum input voltage of 3.3 V for the Nucleo card. Finally, the differential operational amplifier circuit is utilized to scale the signal to the ADC, ensuring accurate measurements and reliable operation of the voltage divider.

From fundamental electrical theory it is known that the voltage drop across a resistor in series with three others can be calculated using Equation 5.1.

$$U_4 = \frac{R_4}{R_1 + R_2 + R_3 + R_4} \tag{5.1}$$

To establish a foundation, $R_1 = R_2 = R_3 = 500\,\text{k}\Omega$, $V_1 = [0 - 1000\,\text{V}]$, $V_4 = [0 - 2\,\text{V}]$ were chosen for the circuit, where the last resistor is determined using Equation 5.2.

$$\begin{aligned} R_4 &= U4 \cdot \frac{R_1 + R_2 + R_3}{U_1 - U_4} \\ &= 2\,\mathrm{V} \cdot \frac{500\,\mathrm{k\Omega} + 500\,\mathrm{k\Omega} + 500\,\mathrm{k\Omega}}{1000\,\mathrm{V} - 2\,\mathrm{V}} \\ &\approx 3.00\,\mathrm{k\Omega} \end{aligned} \tag{5.2}$$

The simulation results presented in Figure 5.3 confirmed the calculations in Equation 5.2, with the voltage divider connected to 1000 V source, and resistor R_4 having a voltage drop of 2 V.

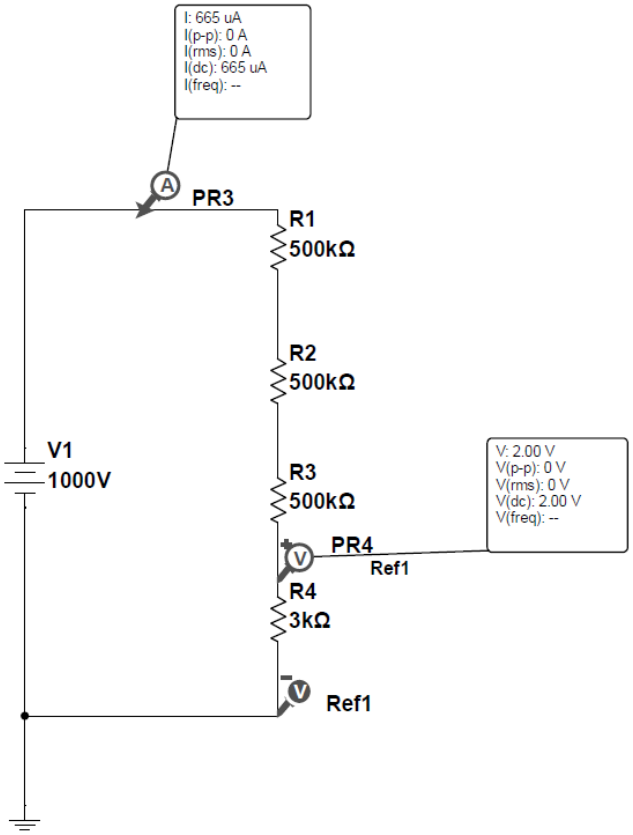


Figure 5.3: Voltage divider (1000 V DC-source).
Source: Screenshot from Multisim.

Furthermore, the current passing through the bridge and power at maximum DC-link voltage (1000 V) are calculated in Equations 5.3, 5.4 and 5.5.

$$\begin{aligned} I_{MAX} &= \frac{U_{MAX}}{R_{TOTAL}} \\ &= \frac{1000\,\mathrm{V}}{500\,\mathrm{k\Omega} + 500\,\mathrm{k\Omega} + 500\,\mathrm{k\Omega} + 3\,\mathrm{k\Omega}} \\ &= 0.665\,\mathrm{mA} \end{aligned} \tag{5.3}$$

$$\begin{aligned} P_{R1_{MAX}} = P_{R2_{MAX}} &= P_{R3_{MAX}} \\ &= I_{MAX}^2 \cdot R \\ &= (0.665\,\mathrm{mA})^2 \cdot 500\,\mathrm{k\Omega} \\ &= 221\,\mathrm{mW} \end{aligned} \tag{5.4}$$

$$\begin{aligned} P_{R4_{MAX}} &= I_{MAX}^2 \cdot R_4 \\ &= (0.665\,\mathrm{mA})^2 \cdot 3\,\mathrm{k\Omega} \\ &= 1.33\,\mathrm{mW} \end{aligned} \tag{5.5}$$

By substituting the nominal DC-link voltage into the corresponding equations used for the maximum DC-link voltage, the resulting values are $I_{nom} = 0.376\,\mathrm{mA}$, $P_{R1_{nom}} = P_{R2_{nom}} = P_{R3_{nom}} = 70.7\,\mathrm{mW}$ and $P_{R4_{nom}} = 0.42\,\mathrm{mW}$.

To summarize, this implies that the resistors in the bridge have to handle at least 221 mW. To add a safety margin, 1206 series resistors should be chosen, capable of handling 0.25 W each. The simulations presented in Figures 5.3 and 5.4 confirms the calculations for maximal operation and nominal operation, respectively.

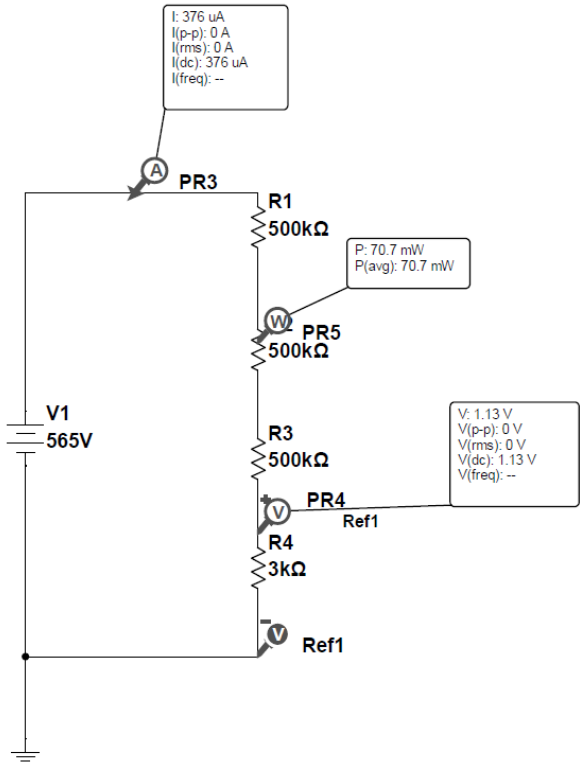


Figure 5.4: Voltage divider (565 V DC-source).
Source: Screenshot from Multisim.

Amplifying to ADC

The isolation amplifier chip has an amplifying ratio 1 : 1. This means 2 V in equals 2 V out. The signal needs to be amplified from $[0 - 2\,\text{V}]$ to $[0 - 3.3\,\text{V}]$, to be able to fully use the ADC's analog input range. To do this, one solution is to implement a differential operational amplifier circuit in the design. This is because the signal from the isolation amplifier is two-wired, $V_{OUT}+$ and $V_{OUT}-$, as presented in Appendix B.11.

Figure 5.5 illustrates an operational amplifier, wired and configured as a differential operational amplifier. If $R_1 = R_2$ and $R_3 = R_3$, the equation describing the output voltage can be simplified as shown in Equation 5.6. Furthermore, Figure 5.6 depicts the typical application of the chosen voltage sensor.

$$V_{OUT} = \frac{R_3}{R_1} \cdot (V_2 - V_1) \tag{5.6}$$

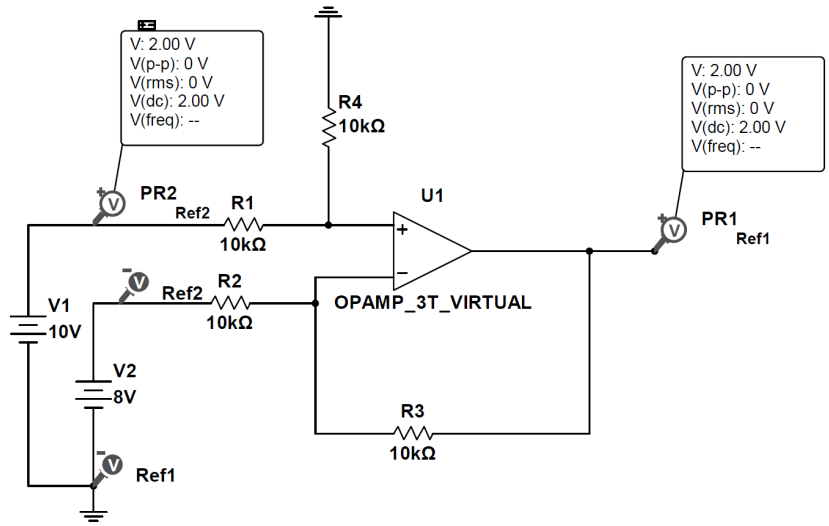


Figure 5.5: Differential operational amplifier.
Source: Screenshot from Multisim.

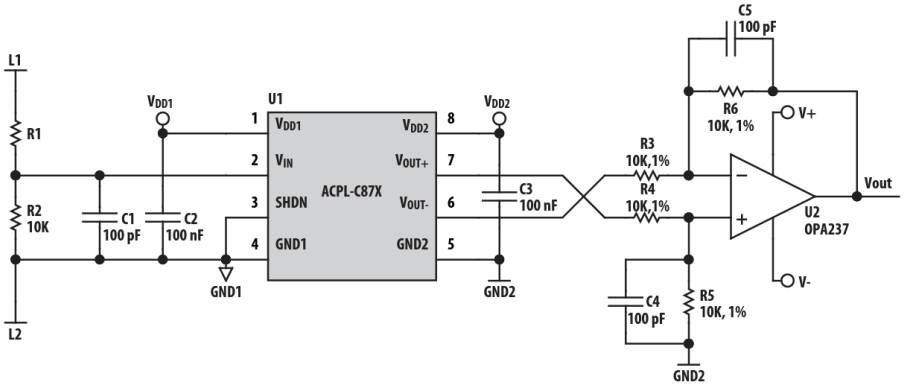


Figure 5.6: Typical application ACPL-C87B-000E.
Source: Screenshot from ACPL-C87B-000E's datasheet.

In this particular scenario, the gain of the operational amplifier is determined by adjusting the value of R_5 and R_6. Based on Figure 5.6, calculating these can be done using Equation 5.7, where $V_{OUT} = 3.3\,\mathrm{V}$, $R3 = R4 = 10\,\mathrm{k\Omega}$ and $V2 - V1 = 2\,\mathrm{V}$.

$$\begin{aligned} R_5 = R_6 &= V_{OUT} \cdot \frac{R_3}{V_2 - V_1} \\ &= 3.3\,\mathrm{V} \cdot \frac{10\,\mathrm{k\Omega}}{2\,\mathrm{V}} \\ &= 16.5\,\mathrm{k\Omega} \end{aligned} \tag{5.7}$$

Figure 5.7 depicts the comprehensive measurement bridge that was devised and simulated in Multisim for measuring the DC-link voltage.

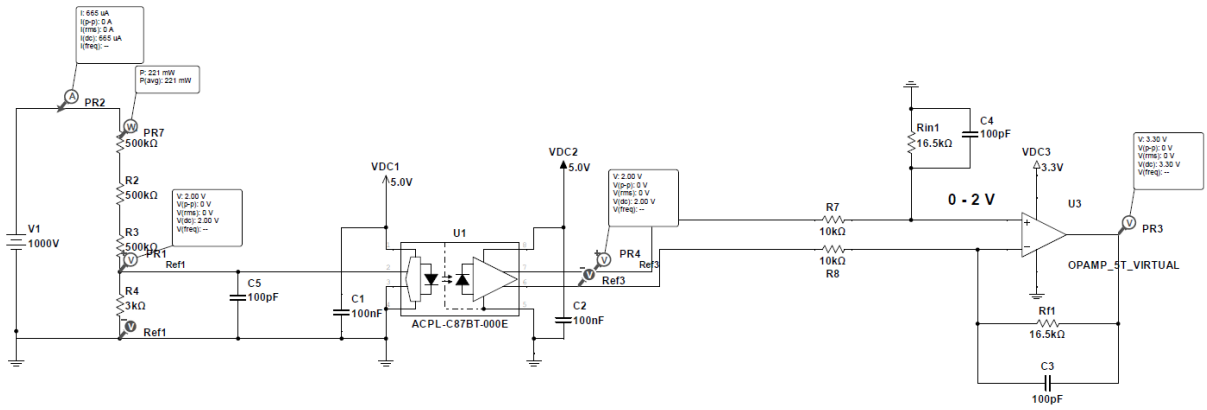


Figure 5.7: Voltage measuring bridge with operational amplifier.
Source: Screenshot from Multisim.

Braking Circuit

As pointed out in Chapter 4.1, a braking circuit is a necessary part of an inverter system where an induction motor may enter regenerative mode. This can cause a voltage increase on the DC-link, which can damage the capacitors and the inverter. To prevent this from happening, a circuit has been designed to measure the DC-link voltage and activate an IGBT that shorts the DC-link through an external load resistor to burn off power and help lower the voltage level. It has been chosen that this safety function should be independent of the microcontroller's operation on the board, meaning it must function without the microcontroller connected or operational. This led to the choice of designing

an analog circuit for comparison between the measured DC-link voltage and a reference that determines when the braking IGBT should switch on or off. A hysteresis has also been designed for the system to ensure that the conditions for switching on and off the IGBT are slightly shifted. This is to prevent it from switching on and off frequently if the DC-link voltage is right at the boundary. The subsystem topology's intended operation is outlined in Figure 5.8.

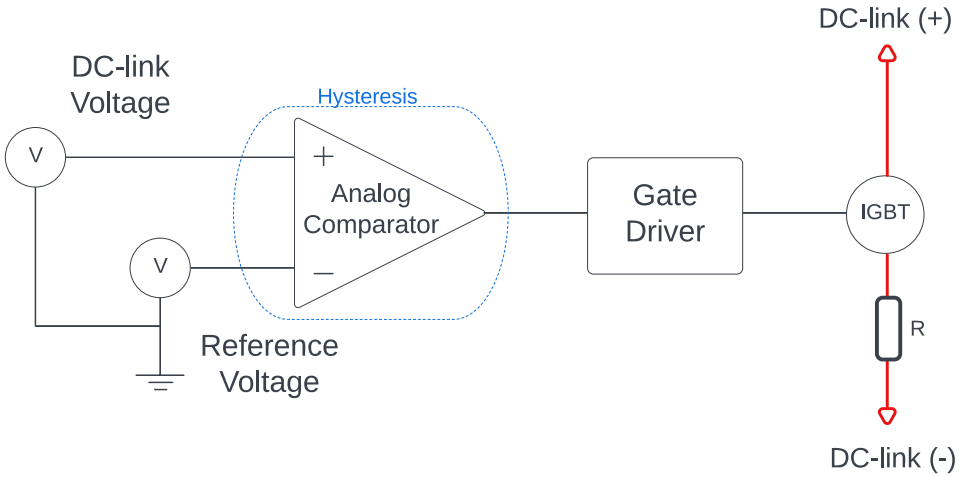


Figure 5.8: Braking circuit topology.
Source: Created using Lucidchart.

Human–Machine Interface

In order to establish an intuitive user interface, it was chosen to implement certain components on the circuit board to serve as the interface between human and machine. This includes a Liquid Crystal Display (LCD), three push buttons and LED diodes. The LCD is integrated in the microcontroller utilizing I2C bus, while the encoder, buttons and LEDs are connected to the microcontroller's input and output pins.

5.3 DC-Link Capacitors

Capacitors play a crucial role in three-phase voltage source inverters, reducing the magnitude of DC-link current and voltage ripples. This leads to the production of smoother and more reliable sinusoidal waveforms with minimal interference. In order to ensure optimal

performance and electromagnetic compatibility of the system, it is essential to minimize the presence of current ripple in the DC-link. This is necessary to prevent the potential generation of Electromagnetic Interference (EMI).

To mitigate these issues, film capacitors are a common choice for this application due to their high power level and low internal resistance, also referred to as ESR, when compared to electrolytic capacitors. While film capacitors are generally more expensive than electrolytic capacitors, they offer higher volume per capacitance, providing a smaller and more straightforward design.

It is important to note that the Root Mean Square (RMS) ripple in the DC-link depends on the power factor, PF, and amplitude modulation index, m_a, which affects the size and selection of the DC-link capacitors.

Calculation of total DC-link capacitance is done using Equation 5.8.

$$\begin{aligned} C_{total} &= \frac{U}{32 \cdot L \cdot \Delta U \cdot f_s^2} \\ &= \frac{565\,\mathrm{V}}{32 \cdot 5\,\mathrm{mH} \cdot 1\,\% \cdot 565\,\mathrm{V} \cdot (5000\,\mathrm{Hz})^2} \\ &= 25\,\mu\mathrm{F} \end{aligned} \tag{5.8}$$

For the design, a voltage ripple of 1 % of U_d from peak to peak is accepted. L is set to 5 mH, which is a value from the datasheet of a standard 3 kW motor. A calculation of the motor equivalent impedance is shown in Appendix B.16. Presented in Figure 5.9 is a graph showing the relationship between voltage ripple and total DC-link capacitance.

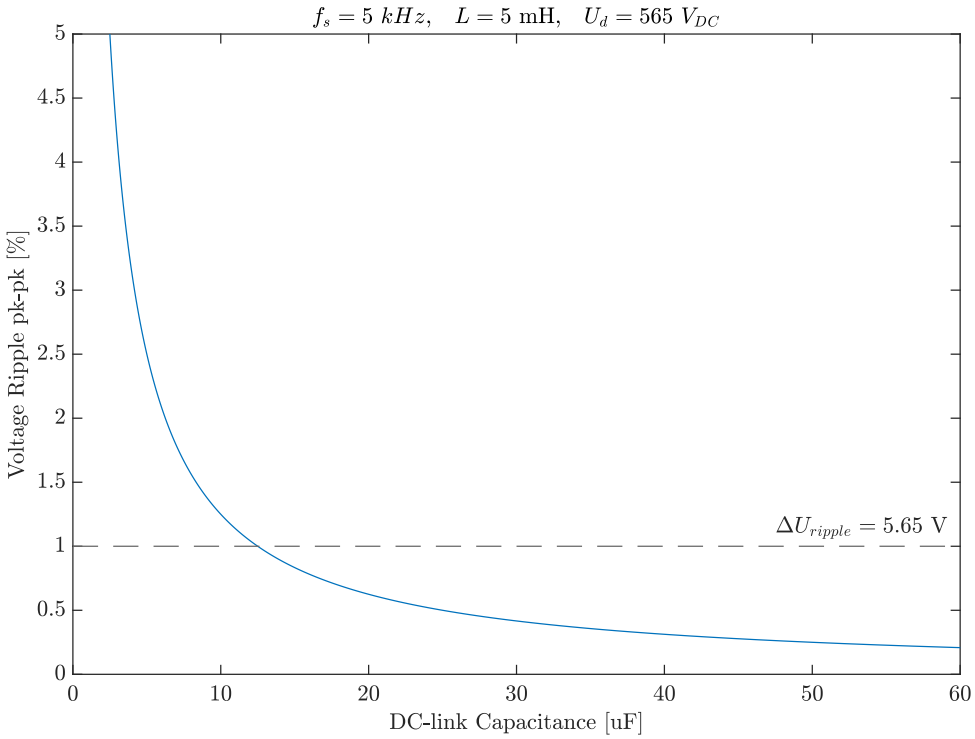


Figure 5.9: Voltage ripple as a function of DC-link capacitance.
Source: Created using MATLAB.

The application is utilizing two film capacitors in series, and therefore total capacitance is divided by two. Between the two capacitors there is a neutral point used for measurements. From Equation 5.9 the chosen capacitor size is 14 µF, and the chosen product was *EPCOS / TDK B32776G0146K000*.

$$\begin{aligned} C1 = C2 &= \frac{C_{total}}{2} \\ &= \frac{25\,\mu\text{F}}{2} \\ &= 12.5\,\mu\text{F} \end{aligned} \tag{5.9}$$

To secure voltage balance between the two capacitors it is necessary to add resistors in parallel with the capacitors. Size of the resistors in parallel with the capacitors is calculated using Equation 5.11. It was decided to use two resistors in series with each capacitor thus multiplying by 1/2. Before calculating the needed resistance a couple correlations needs to be enlightened.

$$u_c(t) = U_{C_0} \cdot e^{-\frac{t}{\tau}} \tag{5.10}$$

It is known that $t = 5 \cdot \tau$. By substituting τ with the product of resistance and capacitance, Equation 5.11 can be used to find the size of one resistor [3, p. 686]. Discharging time for the capacitor, t, is set to 60 seconds.

$$\begin{aligned} R &= \frac{t}{5 \cdot C} \cdot \frac{1}{2} \\ &= \frac{60\,\mathrm{s}}{5 \cdot 14\,\mu\mathrm{F}} \cdot \frac{1}{2} \\ &= 428\,\mathrm{k\Omega} \end{aligned} \tag{5.11}$$

A control of the power developed in one of the DC-link balancing resistors is done in Equation 5.12. The power developed in a single resistor can not exceed the maximum rating for 1206 components which is approximately 0.25 W.

$$\begin{aligned} P &= \frac{U^2}{R} \\ &= \frac{(\frac{565\,\mathrm{V}}{4})^2}{428\,\mathrm{k\Omega}} \\ &= 50\,\mathrm{mW} \end{aligned} \tag{5.12}$$

RMS current is calculated with Equation 5.13.

$$\begin{aligned} I_{ripple_{RMS}} &= \frac{0.25 \cdot U}{2 \cdot \sqrt{2} \cdot fs \cdot L} \\ &= \frac{0.25 \cdot 565\,\mathrm{V}}{2 \cdot \sqrt{2} \cdot 5\,\mathrm{kHz} \cdot 5\,\mathrm{mH}} \\ &= 2\,\mathrm{A} \end{aligned} \tag{5.13}$$

Based on the datasheet for the chosen component *EPCOS / TDK B32776G0146K000*, the maximum RMS current value is specified as 13.5 A. Equation 5.13 predicts an RMS

current value not exceeding 2 A. Therefore, the chosen component meets the requirements for maximum RMS current, and is a suitable option for the application [5].

Although this method is sufficient for this application, DC-link capacity can be calculated in other ways, including a more accurate method using a 3D-plot and equations for minimum capacitance and ripple in current [12].

5.4 PCB Topology Optimization

Following the completion of the work elaborated in Chapter 5.2, the next step involves designing the layout of the PCB. This process necessitates the collection of all essential data related to the component and circuits, which will be utilized to construct a final design that can be forwarded to the production phase. The primary objective of this endeavor is to determine the optimal placement of each individual component on the board, as well as to pinpoint the precise location of the copper traces that interconnect them.

The printed circuit board contains numerous components, each with their own distinct manufacturer-specific design. To facilitate the integration of these components onto the board, data for each component was obtained from Octopart Electronic Component Search Engine [18]. In cases where data was unavailable, the symbols and footprints were created from scratch. All of the symbols, footprints and 3D models have been consolidated in the KiCad project library, which are accessible from the hyperlink provided in Appendix B.

Circuit Board Layout and Galvanic Isolation

In order to maintain a safe and reliable operation, it is imperative to establish a physical separation between the microcontroller low-voltage section of the PCB and the high-voltage section where the IGBTs are situated. This is accomplished by partioning the board into two distinct sections, each marked by lines on the silkscreen, indicating the separation.

The placement of critical components, such as the gate drivers, played a pivotal role in

determining the location of this separation. Specifically, on one side of the board, the IGBTs, main power traces, current sensors, and connection terminals to the DC-link and motor are located, while on the other side contains the microcontroller and other low voltage circuits.

In order to ensure galvanic isolation between the two sections of the board, the galvanic separation has been attempted to be placed in the physical section of the board where gate drivers, 5 V isolated chip and the isolation amplifier chip for voltage measurement are located. However, the placement of the current sensors proved to be a challenge. Three signals in addition to power supply needs to be routed between the sensor and the microcontroller. The current sensors must be placed in the main power section of the board, where they are galvanically isolated internally, to maintain safety. The challenge arises when routing these signals back to the microcontroller while maintaining physical separation between the high and low voltage sections of the board. The solution to this challenge was to implement pins on the board and route all signals through external wires. This was done to avoid routing the signals through the power section of the inverter, which would violate the principles of galvanic isolation and physical separation between high voltage and low voltage components.

Copper Tracing to the Microcontroller

The circuit board features a microcontroller that boasts versatile interfaces for controlling, measuring and monitoring the various systems within the design. However, due to multifaceted nature of these interfaces, the microcontroller necessitates connections to multiple locations across the board, which can make routing the copper traces a challenging task. To streamline this process, it has been taken a methodical and structured approach to implementation, seeking to minimize the use of vias and crossings wherever possible and routing signals in parallel wherever practical. The microcontroller itself operates on 3.3 V logic, while the applied gate drivers utilize 5 V logic. To ensure seamless communication between these components, level shifters have been employed to translate the signals between the two voltage levels. Therefore, every signal that travels to and from the gate driver, must pass through a level shifter chip to enable effective and correct transmission.

Significant efforts to optimize the implementation of the microcontroller and associated components on the board have been done to assure correct operation.

Optimization of PCB Area

To minimize the use of space on a circuit board, it is crucial to effectively distribute components across both the front and back sides of the board. The board has two copper layers available for routing copper traces. Most of the components used are Surface Mount Devices (SMDs), meaning that the side of the board they are placed on is the side of which the component is soldered to. Great effort has been made to make optimal choices for component placement, ensuring that all copper traces can be routed without conflicts while also keeping components that need to be interconnected close together to minimize trace lengths. While some consideration has been given to reducing the size of the design's size, functionality has remained the top priority. Nevertheless, the design has undergone several iterations and has been reduced somewhat in size. Future iterations, however, have the potential to achieve significant size reduction while maintaining optimal functionality.

Copper Trace Capacity

JLCPCB has been selected as the supplier of the circuit board. The two copper layers of the circuit board can be ordered with either 1 oz or 2 oz copper weight, which refers to the thickness of each copper layer. The supervisor intends to use the 1 oz option as it is the most cost-effective alternative. Calculations must be performed to determine the width of the main power copper traces to handle the current flowing through it.

The standard thickness of the copper traces for standard applications is 1 oz, which corresponds to a thickness of 1.4 mils = 0.0356 mm. In KiCad 6.0, there is a implemented tool called PCB Calculator that can calculate the current-carrying capability of a copper trace. The calculations are based on Equation 5.14, where I is maximal currents in ampere, ΔT is the temperature rise above ambient in degree Celsius, W is the copper trace width in mils, H is copper trace thickness in mils, and K is 0.024 for internal tracks or 0.048 for

external tracks.

$$I = K \cdot \Delta T^{0.44} \cdot (W \cdot H)^{0.725} \tag{5.14}$$

Solving 5.14 for W with $I = 5\,\text{A}$, $\Delta T = 40\,^{\circ}\text{C}$, $H = 1.4\,\text{mils}$ and $K = 0.048$ results in Equation 5.15.

$$\begin{aligned} W &= \frac{\left(\frac{I}{K \cdot \Delta T^{0.44}}\right)^{\frac{40}{29}}}{H} \\ &= \frac{\left(\frac{5}{0.048 \cdot 40^{0.44}}\right)^{\frac{40}{29}}}{1.4} \\ &= 46.20\,\text{mils} = 1.17\,\text{mm} \end{aligned} \tag{5.15}$$

Calculations done in Equation 5.15 indicates that the main copper traces need to be a minimum of 1.17 mm to carry 5 A. In the final design, 8 mm main tracks were provided, making the inverter max output current being 20 A regarding copper trace dimensions.

Chapter 6

Temperature Control

Effective temperature control is a critical aspect in power electronics to safeguard electrical components, especially semiconductors, from potential damage. Overheating can for instance lead to reduced component lifespan or increased leakage current. Therefore it is crucial to operate within the specified temperature range for each component. A heat sink is a good solution for dissipating heat and staying within the temperature range with a good margin [3, p. 730].

6.1 Thermal Dissipation Analysis

All electric components generate heat during operation. To maintain the specified range of temperature for the components it is necessary to consider the power losses in each critical component.

In this application there are six transistors. Preventing overheating of the transistors is extra important with them being semiconductors. Calculating power dissipation of the transistor consists of losses from Insulated-Gate Bipolar Transistor (IGBT) and diode. These calculations are mainly comprised by steady-state conduction losses, P_{cond}, and switching losses, P_{sw}. Leakage losses, P_{leak}, in both IGBT and diode are small enough to be neglected [11].

Total power dissipation of IGBT and antiparallell diode is shown in Equation 6.1 [15]. All values used in the following equations are from the datasheet of the IGBT *Infineon IKW40N120H3*. Gate resistance, R_{gate}, is proportional to power dissipation. In the IGBT's datasheet all values are based on R_{gate} being set to $12\,\Omega$. Calculations are done in MATLAB, and presented in Appendix D.9.

$$\begin{aligned} P_d = P_{cond} + P_{sw} + P_{leak} &\approx P_{cond} + P_{sw} \\ &= P_{IGBT} + P_{diode} \\ &= P_{cond_{IGBT}} + P_{sw_{IGBT}} + P_{cond_{diode}} + P_{sw_{diode}} \end{aligned} \tag{6.1}$$

Heat Generation of Transistors

As discussed in Chapter 5.2 the transistor chosen for this application is *Infineon IKW40N120H3*. To prevent thermal runaway in high power IGBT modules, it is necessary to implement an appropriate heat sink, which can efficiently dissipate the heat generated during operation [15, p. 2].

Power loss calculations for IGBT consists of conduction loss, switching loss and a small leakage loss, whereof the latter is neglected. Equations for conduction loss and switching loss in IGBT are shown in Equation 6.2 and 6.3.

Saturation voltage between collector and emitter in IGBT, $U_{CE_{SAT}}$, is the voltage between collector and emitter under the given conditions. Duty cycle, D, is the relationship between time on and time off in the IGBT. Total switching energy, E_{ts}, is the total energy dissipated in the IGBT due to switching [15, p. 3].

$$\begin{aligned} P_{cond_{IGBT}} &= U_{CE_{SAT}} \cdot I_c \cdot D \\ &= 1.8\,\mathrm{V} \cdot 5\,\mathrm{A} \cdot 50\,\% \\ &= 4.5\,\mathrm{W} \end{aligned} \tag{6.2}$$

$$\begin{aligned} P_{sw_{IGBT}} &= E_{ts} \cdot f_s \\ &= 1.3\,\text{mJ} \cdot 5\,\text{kHz} \\ &= 6.5\,\text{W} \end{aligned} \tag{6.3}$$

Heat Generation of Diodes

The chosen transistor has a built-in anti-parallel diode. Losses in the diode is given by forward conduction loss and switching loss. Switching loss in diode is also referred to as reverse recovery loss [3, p. 535].

Calculating conduction loss in the diode requires values from a graphs given in the datasheet for the component *Infineon IKW40N120H3*. On-state voltage, U_{D_0}, and on-state resistance, R_D, are found in Figure 6.1 and calculated in Equation 6.4 [15, p. 3].

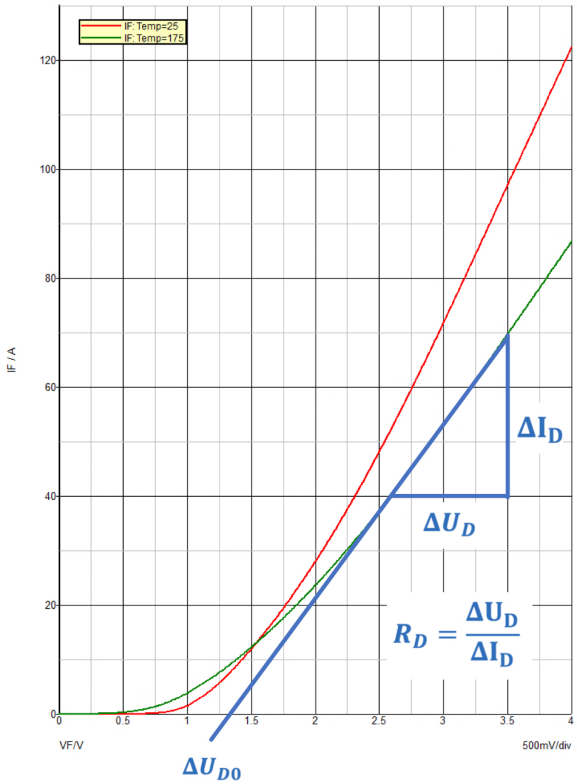


Figure 6.1: Typical diode forward current as a function of forward voltage.
Source: Screenshot from IKW40N120H3's datasheet.

$$\begin{aligned} R_D &= \frac{\Delta U_D}{\Delta I_D} \\ &= \frac{3.5\,\mathrm{V} - 2.6\,\mathrm{V}}{70\,\mathrm{A} - 30\,\mathrm{A}} \\ &= 22.5\,\mathrm{m\Omega} \end{aligned} \tag{6.4}$$

RMS current through the diode in forward bias, $I_{D_{RMS}}$, is shown in Figure 6.2 and the calculation is shown in Equation 6.5 [14].

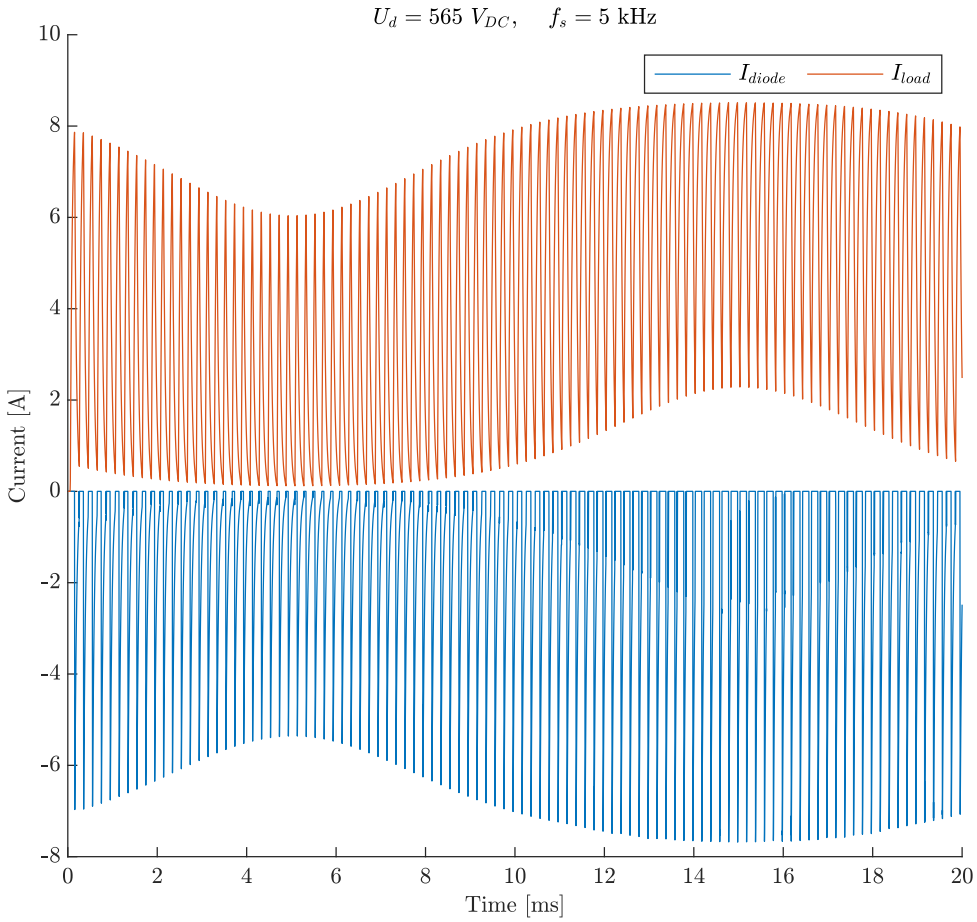


Figure 6.2: Diode current in nominal operation.
Source: Created using MATLAB (data from LTspice).

$$\begin{aligned} I_{D_{RMS}} &= \sqrt{(\frac{1}{2} + D) \cdot \frac{I_C^2}{4} - \frac{m_a \cdot \cos\phi \cdot I_C^2}{3 \cdot \pi}} \\ &= \sqrt{(\frac{1}{2} + 50\,\%) \cdot \frac{(5\,\mathrm{A})^2}{4} - \frac{0.5 \cdot 0.7 \cdot (5\,\mathrm{A})^2}{3 \cdot \pi}} \\ &= 2.3\,\mathrm{A} \end{aligned} \tag{6.5}$$

$$\begin{aligned} P_{cond_{Diode}} &= (U_{D_0} \cdot I_{D_{RMS}} + R_D \cdot I_{D_{RMS}}^2) \cdot D \\ &= (1.35\,\mathrm{V} \cdot 2.3\,\mathrm{A} + 22.5\,\mathrm{m\Omega} \cdot (2.3\,\mathrm{A})^2) \cdot 50\,\% \\ &= 1.62\,\mathrm{W} \end{aligned} \tag{6.6}$$

Switching loss in diode is calculated from the reverse recovery energy, E_{rec}, in the diode. Figure 6.3 shows the reverse recovery current in the diode.

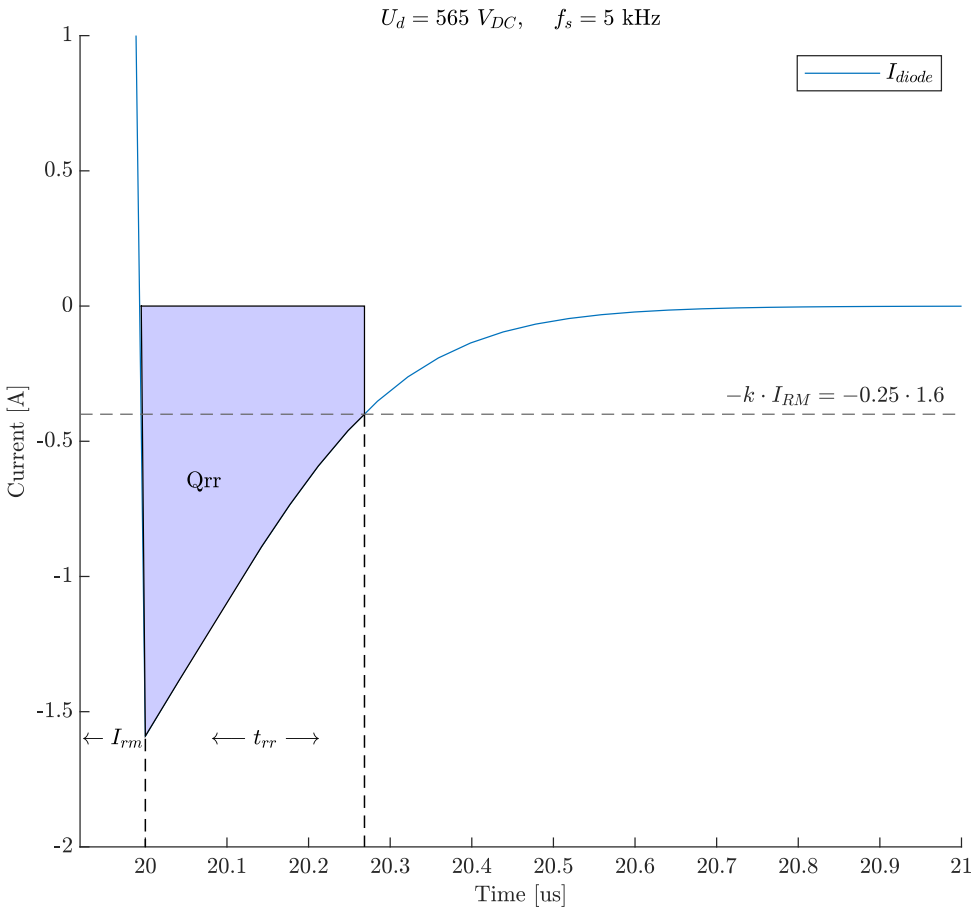


Figure 6.3: Reverse recovery current in diode.
Source: Created using MATLAB (data from LTspice).

Reverse recovery current, I_{rm}, is the minimum current value the diode reaches while in reverse recovery. Reverse recovery time, t_{rr}, is the time from the dip in current reaches zero untill it reaches $-0.25 \cdot I_{rm}$. The reason for this dip is that the diode goes from forward bias to reverse bias [3, p. 538]. The datasheet for the chosen IGBT only contain values for diode at nominal operation, which is 40 A and 600 V. Equation 6.7 uses values measured at nominal operation, and in Equation 6.8 it is taken care of by multiplying by the relationship between nominal and chosen operating point [16].

$$\begin{aligned} E_{rec_{nom}} &= P \cdot t \\ &= U_D \cdot I_{rm} \cdot t_{rr} \\ &= 565\,\mathrm{V} \cdot 16\,\mathrm{A} \cdot 639\,\mathrm{ns} \\ &= 5.8\,\mathrm{mJ} \end{aligned} \tag{6.7}$$

$$\begin{aligned} P_{sw_{diode}} &= E_{rec_{nom}} \cdot f_s \cdot \frac{\sqrt{2} \cdot I_{RMS}}{\pi \cdot I_{nom}} \cdot \frac{U_D}{U_{nom}} \\ &= 5.8\,\mathrm{mJ} \cdot 5\,\mathrm{kHz} \cdot \frac{\sqrt{2} \cdot 5\,\mathrm{A}}{\pi \cdot 40\,\mathrm{A}} \cdot \frac{565\,\mathrm{V}}{600\,\mathrm{V}} \\ &= 1.53\,\mathrm{W} \end{aligned} \tag{6.8}$$

$$\begin{aligned} P_{diode} &= P_{cond} + P_{sw} \\ &= 1.62\,\mathrm{W} + 1.53\,\mathrm{W} \\ &= 3.15\,\mathrm{W} \end{aligned} \tag{6.9}$$

Total power dissipation is calculated in Equation 6.10 and is used in further calculations of heat sink dimensions.

$$\begin{aligned} P_d &= P_{IGBT} + P_{diode} \\ &= 11\,\mathrm{W} + 3.15\,\mathrm{W} \\ &= 14.15\,\mathrm{W} \end{aligned} \tag{6.10}$$

Impact of Switching Frequency

Studies have revealed that the human auditory system is capable of perceiving frequencies in the range of 20 Hz to 20 kHz on average [6, p. 1]. Consequently, it is recommended

to utilize switching frequencies exceeding 20 kHz when triggering the transistors. This is also conducive to a simpler design for noise filters, such as LC low pass filters. However, higher switching frequencies are accompanied by an increase in power dissipation, thus necessitating a cost-benefit analysis. Mathematically, switching frequency is proportional to power dissipation in the transistor and inverse proportional to the size of the LC-filter on the output. From Equation 5.8 in Chapter 5 it is shown that L is inversely proportional to switching frequency.

Considering power dissipation, switching frequency should be as low as possible to avoid a big heat sink, high costs and major power losses. Considering the LC filter, switching frequency should be as high as possible to avoid high costs for the filter. In other words, it is needed to find the best operating point that does not cause too much power dissipation and simultaneously not causing the costs for LC filter to become too high. Taking both the noise from switching and calculations of power dissipation and LC-filter in consideration, it has been determined that the inverter is to operate at nominal operating conditions with a switching frequency, f_s, of 5 kHz. In Figure 6.4 the proportional relationship between switching frequency and power dissipation is demonstrated.

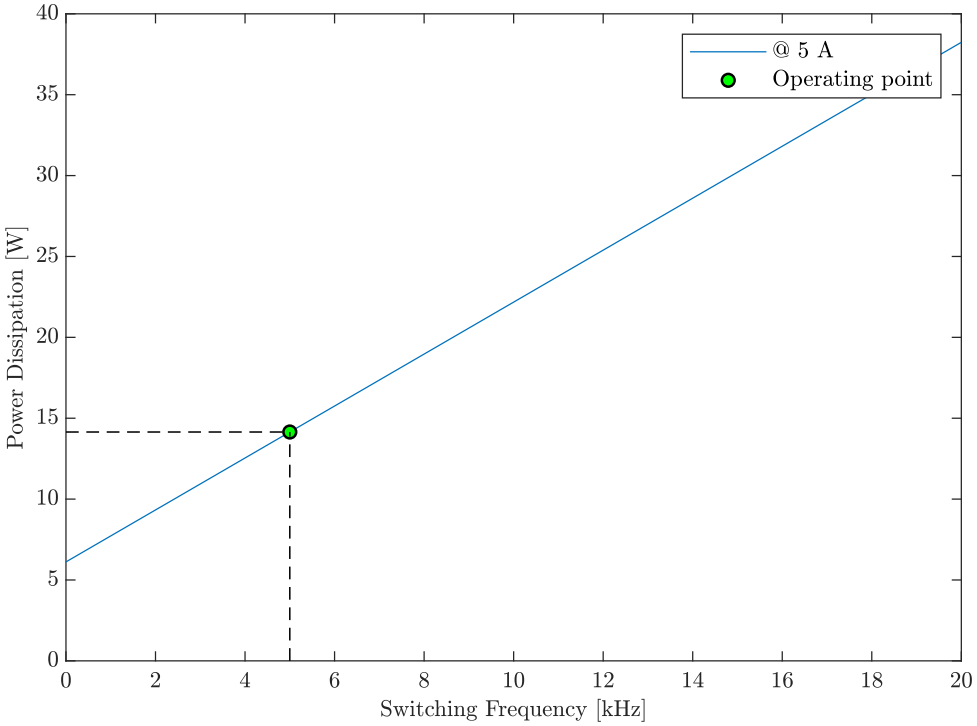


Figure 6.4: Power dissipation as function of switching frequency.
Source: Created using MATLAB.

6.2 Thermal Calculations

The total power dissipation calculated in section 6.1 needs to be dissipated with a heat sink to avoid overheating. Without a heat sink the transistor gains 40 °C per dissipated watt, according to the datasheet for the chosen transistor. This results in overheating without a proper way to dissipate the heat. In order to dissipate enough heat it is necessary to calculate thermal resistance, $R_{\theta sa}$, which decides the geometric size of the heat sink. The lower the total thermal resistance is, bigger heat sink is required [3, p. 738]. Therefore it is crucial to find components making total thermal impedance as great as possible. This is to save space on the circuit board, and to lower costs of the heat sink.

The thermal resistance from the heat sink to the ambient air, $R_{\theta sa}$, can be calculated using Equation 6.11. Maximum temperature for the transistor, T_j, is specified in the datasheet (*Infineon IKW40N120H3*) as 175 °C. Ambient temperature, T_a, has been established as 40 °C, as this represents the most severe operating condition for the given application. Thermal resistance from the junction to the transistor, $R_{\theta jc}$, and thermal resistance between the transistor and heat sink, $R_{\theta cs}$, is calculated in the following subsections.

$$R_{\theta sa} = \frac{T_j - T_a}{P_d} - (R_{\theta jc} + R_{\theta cs}) \tag{6.11}$$

Junction-Case Thermal Resistance

The thermal resistance from the junction to the case in the transistor is calculated using Equation 6.12 [15, p. 6]. Thermal resistance from junction to case in the IGBT, $R_{\theta jc_{IBGT}}$, and diode, $R_{\theta jc_{diode}}$, are given in the datasheet for the transistor (*Infineon IKW40N120H3*).

$$\begin{aligned} R_{\theta jc} &= \frac{R_{\theta jc_{IGBT}} \cdot R_{\theta jc_{diode}}}{R_{\theta jc_{IGBT}} + R_{\theta jc_{IGBT}}} \\ &= \frac{0.31\,\mathrm{K/W} \cdot 1.1\,\mathrm{K/W}}{0.31\,\mathrm{K/W} + 1.1\,\mathrm{K/W}} \\ &= 0.2418\,\mathrm{K/W} \end{aligned} \tag{6.12}$$

Thermal Pad Resistance

Thermal pads are used to provide a thermally conductive interface between two surfaces, such as a heat sink and a transistor. The thermal conductivity of the pad, measured in W/mK, determines how well it can transfer heat from one surface to the other. A higher thermal conductivity generally means better heat transfer and therefore better cooling performance [3, p. 737].

It is important to note that other factors, such as the surface roughness of the two surfaces being joined, the pressure applied to the thermal pad, and the ambient temperature can also affect the thermal performance of a thermal pad [3, p. 738]. The pad used in this application, *Wakefield-Vette CD-02-05-247*, has a thermal impedance of 0.107 K/W.

The thermal resistance from the heat sink to ambient air is calculated with Equation 6.13 and further on it is possible to choose a heat sink [3, p. 732].

$$\begin{aligned} R_{\theta sa} &= \frac{T_j - T_a}{P_d} - (R_{\theta jc} + R_{\theta cs}) \\ &= \frac{175\,^\circ\text{C} - 40\,^\circ\text{C}}{14.15\,\text{W}} - (0.2418\,\text{K/W} + 0.107\,\text{K/W}) \\ &= 9.13\,\text{K/W} \end{aligned} \tag{6.13}$$

From the calculations, the heat sink should be 9.13 K/W, or smaller. Lower thermal resistance leads to better heat dissipation. The chosen heat sink is a double heat sink with a minimum thermal resistance at 6 K/W, *Ohmite C247-075-3AE*. The performance of the heat sink is better with forced cooling [3, p. 737]. A calculation of thermal resistance using the dimensions of the chosen heat sink is shown in Appendix D.9 [3, p. 739-742]. Figure 6.5 shows the relationship between power dissipation and the heat sink size.

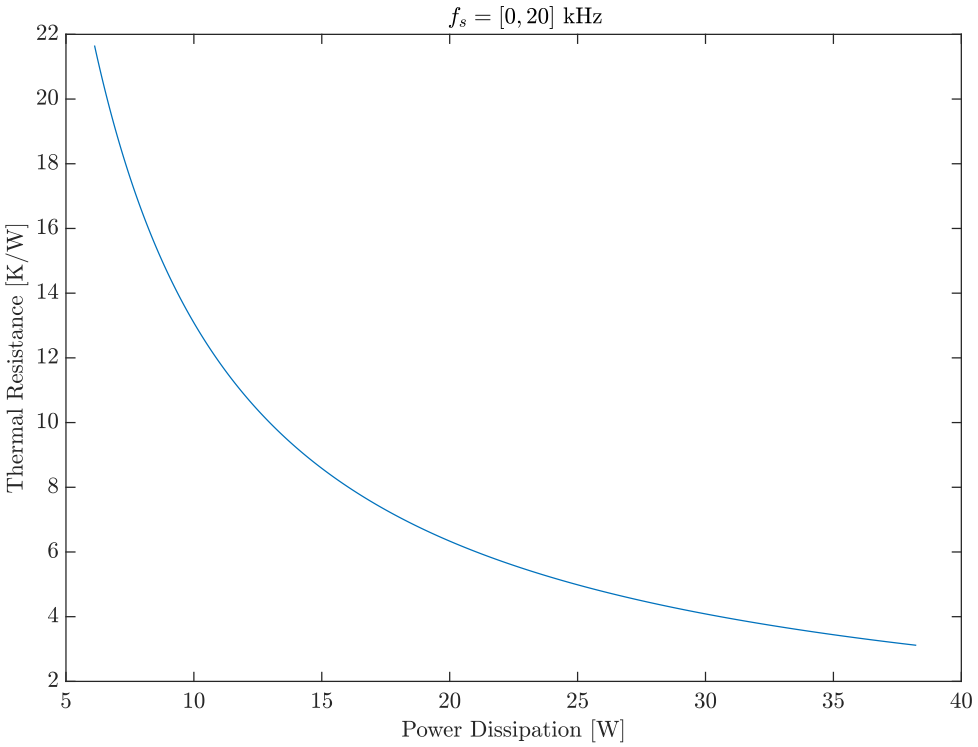


Figure 6.5: Thermal resistance as a function of power dissipation.
Source: Created using MATLAB.

Chapter 7

Software Development

In accordance with the problem analysis outlined in Chapter 4, the selection of a 32-bit STM microcontroller has been established. Following research and consultation with the project supervisor, it is determined that the NUCLEO-L476RG development board is the most appropriate choice for this project. The aforementioned board satisfies all requisite criteria, including the provision of a minimum number of I/O with support for Pulse Width Modulation (PWM), analog input functionality, and advanced timers necessary for motor control.

7.1 Abstraction Layers

The STM family of 32-bit flash MCUs, based on the ARM Cortex-M processor, has been specifically engineered to provide MCU users with unparalleled levels of flexibility [19]. These microcontrollers provide various programming options, with the Hardware Abstraction Layer (HAL) and the Low-Level (LL) library being the two primary software libraries. Nevertheless, both these libraries have distinct advantages and disadvantages.

The HAL library provides a high-level abstraction of the microcontroller's hardware, thereby facilitating easy access to its features. The library proffers a comprehensive array of functions that is straightforward to use. However, its performance may be marginally

inferior to that of the LL library [20, p. 7].

The LL library accords direct access to the microcontroller's hardware, thereby conferring complete control over its features, which generally outstrips the HAL library in terms of performance. However, exploiting this library necessitates a profound comprehension of the microcontroller's hardware, and may require a greater investment of time to use efficiently [20, p. 2566].

In the present project, it is determined that the implementation of various modulation algorithms, especially the Space Vector Pulse Width Modulation algorithm, necessitated the use of the LL library. This decision was made in order to mitigate potential timing-related challenges that may arise in the implementation of the aforementioned algorithm, which is more complex in nature.

7.2 Timer Parameters

As discussed in Chapter 2.1, inverters rely on Pulse Width Modulation (PWM) to convert DC to AC, where a triangular waveform is the basis for the different modulation algorithms. In the context of microcontrollers, PWM timers are used to generate this waveform. A relationship between the a system clock frequency, f_{system}, a prescaler, $k_{prescale}$, a timer clock frequency, f_{timer}, an auto reload parameter, k_{reload}, and a comparison value, $k_{compare}$, determines the time interval between each output trigger and the resulting duty cycle, D. The relationship between these parameters can be expressed by the following equations:

$$f_{timer} = \frac{f_{system}}{k_{prescale}} \tag{7.1}$$

$$f_s = \frac{f_{timer}}{k_{reload}} \tag{7.2}$$

$$D = \frac{k_{compare}}{k_{reload}} \cdot 100\,\% \tag{7.3}$$

The interdependence among these parameters is depicted in Figure 7.1, wherein an output signal is generated to control a given transistor, T_{X+}, in the context of the inverter shown in Figure 2.1. It is also noteworthy to mention that the auto reload parameter has been set to the maximum value of the 16-bit timer utilized in the project, which is limited by an unsigned integer of 65 536. This configuration has been done to maximize the resolution, thereby enhancing accuracy of the comparisons.

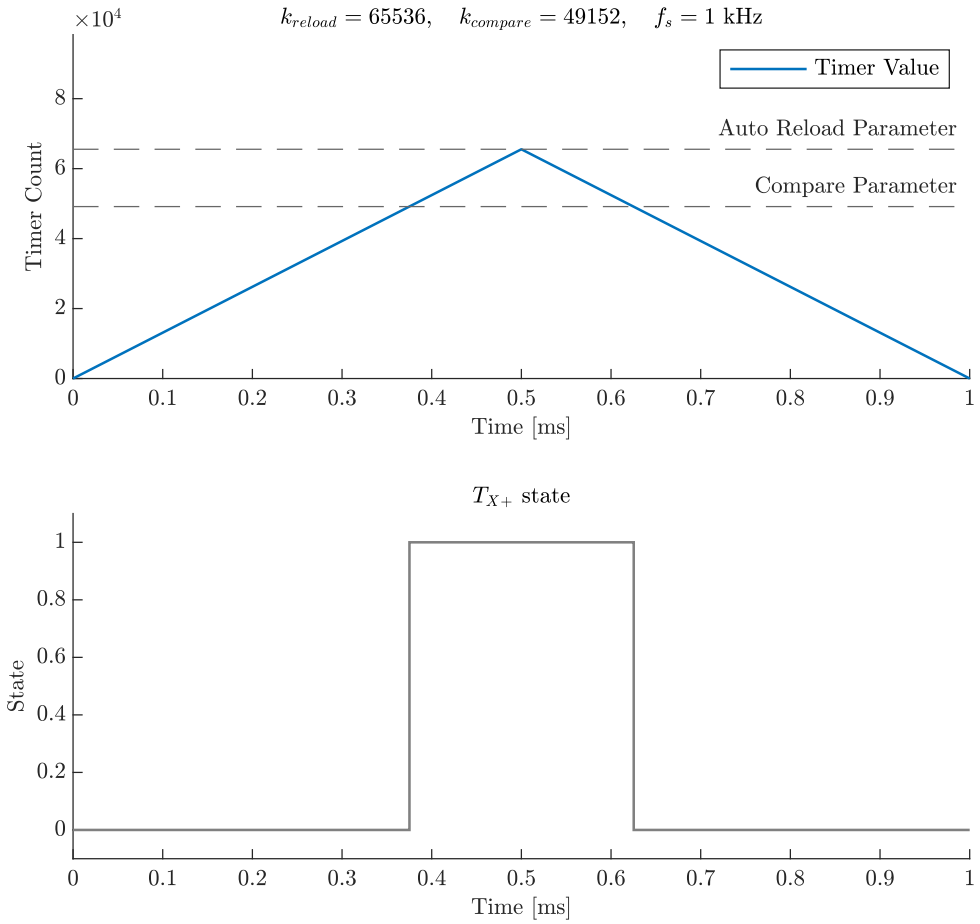


Figure 7.1: Working principle of the microcontroller's embedded PWM timers.
Source: Created using MATLAB.

The signal has been generated under a switching frequency of 1 kHz and illustrates a compare value of 49 152, which when substituted into Equation 7.3 results in a duty cycle

of 75 %:

$$\begin{aligned} D &= \frac{k_{compare}}{k_{reload}} \cdot 100\,\% \\ &= \frac{49152}{65536} \cdot 100\,\% \\ &= 75\,\% \end{aligned} \tag{7.4}$$

By changing the compare values several times in a short period, one can achieve control signals for any geometric shape. The microcontroller chosen for this project also supports more than one compare value per timer, which means that the triangular wave can be compared to more than one control signal, implying multiple geometric shapes. This is necessary when designing an inverter.

7.3 Implementation of Modulation Algorithms

In accordance with the requirement specification presented in Table 3.1, the inverter is required to function utilizing a rectified AC voltage, or specifically, a DC-link voltage in the range of 565 $\mathrm{V_{DC}}$ to 1000 $\mathrm{V_{DC}}$. The modulation algorithms employed by the inverter should facilitate modulation of an AC line voltage at 400 $\mathrm{V_{RMS}}$ with a modulation frequency, denoted as f_1, ranging from 50 Hz to 100 Hz. Furthermore, the inverter should be able to operate at switching frequencies of 5 kHz, as determined in Chapter 6.1.

Considering the aforementioned conditions, the subsequent subsections will demonstrate the design of the program code utilized by the microcontroller in the project, with particular emphasis on the implementation of the algorithms. A segment of the inverter's program code has been replicated in Appendix C, while the all-encompassing code for the inverter is accessible via the hyperlink provided therein. Additionally, a deviation log has been appended in Appendix C.3.

Sinusoidal PWM Signal Generation

In the course of this project's inverter development, the intended modulation technique shall use the Space Vector Pulse Width Modulation algorithm. However, to facilitate comparative analysis during laboratory experiments, the inclusion of an alternative algorithm has been deemed appropriate. Consequently, the chosen alternative is the Sinusoidal Pulse Width Modulation (SPWM) algorithm, which, as per the theoretical discussion presented in Chapter 2.2, is based on comparing a sinusoidal control signal, $U_{control}$, with a triangular carrier signal, U_{tri}, to generate an AC voltage.

To represent the carrier signal within the microcontroller, embedded timers can be utilized. According to the microcontroller's datasheet, the maximum operating system clock frequency is 80 MHz [21, p. 1]. As described in Section 7.2, there exists a correlation between the system clock frequency and the timer frequency. Given that there is no apparent rationale for reducing the counting speed of the timer, it is set to be equal to the system clock frequency, which results in $f_{timer} = f_{system} = 80\,\text{MHz}$. This establishes a prescaler value of 1, as can be seen of Equation 7.1. Utilizing these conditions, the amplitude of the carrier signal, k_{reload}, can be determined by substituting the identified values into Equation 7.2:

$$\begin{aligned} k_{reload} &= \frac{f_{timer}}{f_s} \\ &= \frac{80\,\text{MHz}}{5\,\text{kHz}} \\ &= 16\,000 \end{aligned} \tag{7.5}$$

Furthermore, in a three-phase system, the algorithm necessitates the utilization of three control signals, each signifying three phase voltages with a 120-degree displacement. These can be expressed mathematically by the expressions in Equation 7.6.

$$U_{L1_{control}} = \hat{U}_{Xo1} \cdot \sin(\omega_1 \cdot t) \tag{7.6a}$$

$$U_{L2_{control}} = \hat{U}_{Xo1} \cdot \sin(\omega_1 \cdot t - 120°) \tag{7.6b}$$

$$U_{L3_{control}} = \hat{U}_{Xo1} \cdot \sin(\omega_1 \cdot t + 120°) \tag{7.6c}$$

When translating the expressions from Equation 7.6 for implementation in the microcontroller, they are represented by three compare signals as shown in Equation 7.7.

$$U_{L1_{compare}} = \frac{1}{2} \cdot m_a \cdot k_{reload} \cdot \sin(2\pi \cdot f_1 \cdot t) + \frac{bias}{2} \tag{7.7a}$$

$$U_{L2_{compare}} = \frac{1}{2} \cdot m_a \cdot k_{reload} \cdot \sin(2\pi \cdot f_1 \cdot t - 120°) + \frac{bias}{2} \tag{7.7b}$$

$$U_{L3_{compare}} = \frac{1}{2} \cdot m_a \cdot k_{reload} \cdot \sin(2\pi \cdot f_1 \cdot t + 120°) + \frac{bias}{2} \tag{7.7c}$$

where

$$\begin{cases} m_a \leq 1.0, \\ bias = k_{reload} \end{cases}$$

Following the expressions in Equation 7.7, it should be noted that the inclusion of a bias term serves to prevent the occurrence of negative values in the control signals, while the division of each expression by 2 ensures that the resulting values of the control signals do not exceed the auto reload parameter k_{reload}.

Based on the aforementioned definitions, Figure 7.2 visually presents the theoretical outcome in nominal operation by the use of the Sinusoidal Pulse Width Modulation (PWM) algorithm within the linear modulating region and a DC-link voltage of 565 V. The algorithm is utilized to trigger the transistors by detecting the moment when the instantaneous value of the timer clock intersects one of the sinusoidal waves, which are drawn for $f_1 = 50\,\text{Hz}$. This event triggers a change in the state of the associated pin of the timer channel, occurring at a frequency of 5000 times per second.

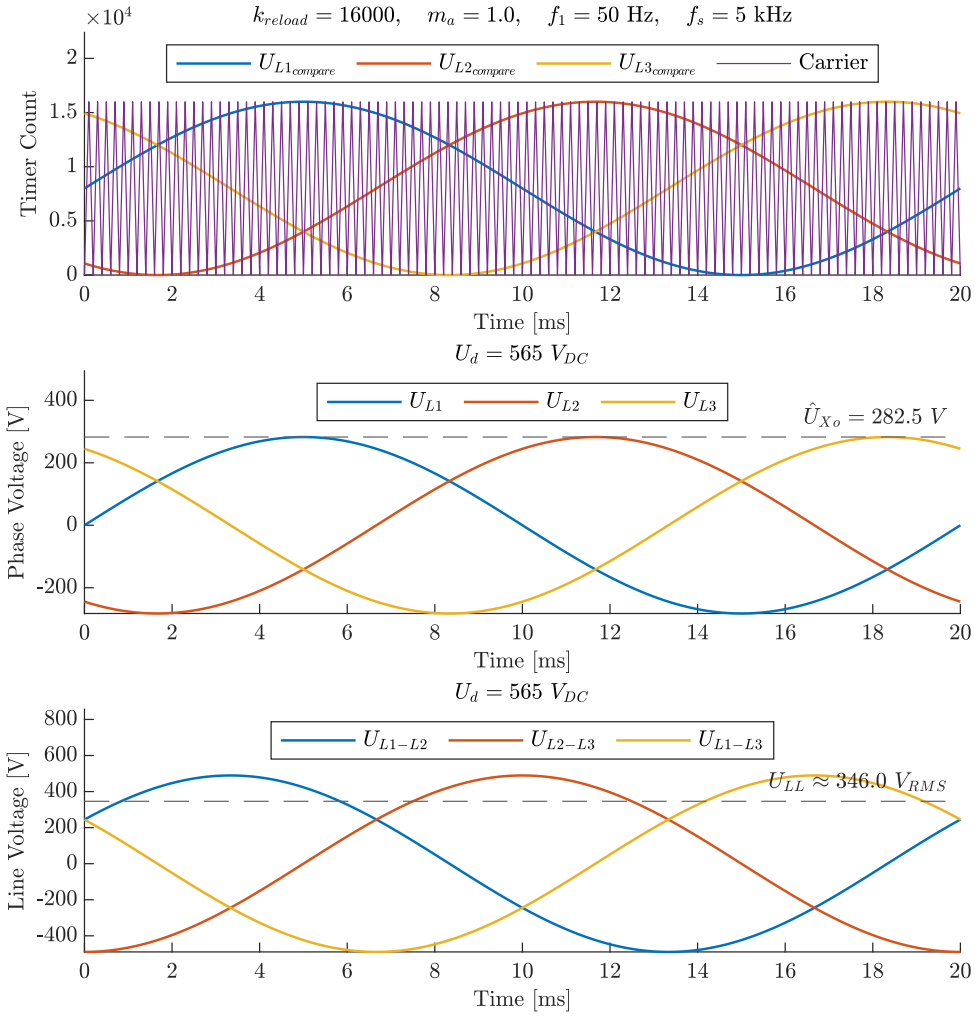


Figure 7.2: Anticipated outcome through the generation of a Sinusoidal PWM modulated signal ($U_d = 565\,\mathrm{V_{DC}}$).
Source: Created using MATLAB.

As observed from the figure, the inverter are able to generate a maximum AC phase voltage of 282.5 V, as determined from Equation 2.9, which corresponds to an output RMS line voltage of approximately 346 V, as calculated from Equation 2.16.

Space Vector PWM Signal Generation

Based on the theory presented in Chapter 2.3, the Space Vector Pulse Width Modulation (SV-PWM) algorithm also relies on a comparison between a sinusoidal control signal and a triangular carrier signal.

The representation of the carrier signal follows the same procedure explained in the previous section on SPWM, where the timer clock frequency is set equal to the system clock frequency, resulting in an amplitude of the carrier signal, k_{reload}, equal to 16 000, as previously calculated in Equation 7.5.

Regarding the three control signals, each signal comprises a fundamental component that resembles the control signal employed in SPWM, alongside a third harmonic component that is distinctive to SV-PWM. As illustrated by Equations 2.17 and 2.16, SV-PWM is capable of synthesizing an output voltage that is $^2/\sqrt{3}$ times greater than that of SPWM. This implies that the fundamental component of the control signal, $U_{LX_{control}}$, utilizing the SV-PWM algorithm can be represented by Equation 7.8.

$$U_{LX_{control}} = \frac{2}{\sqrt{3}} \cdot \overbrace{\hat{U}_{Xo1} \cdot \sin\left(\omega_1 \cdot t + \theta_s\right)}^{\text{Eq. 7.6}} \tag{7.8}$$

Furthermore, it is imperative to incorporate the third harmonic component into the fundamental component. This is achieved by subtracting a proportion of the fundamental component, wherein the magnitude of the share is contingent upon which of the three voltages exhibit the greatest disparity relative to the DC-link voltage [8, p. 124]. Consequently, the three compare values can be expressed as shown in Equation 7.9. Note that the same bias considerations utilized in Equation 7.7 are employed to prevent the compare signals from taking negative values.

$$U_{L1_{compare}} = \overbrace{\frac{1}{\sqrt{3}} \cdot m_a \cdot k_{reload} \cdot \sin\left(2\pi \cdot f_1 \cdot t\right)}^{\text{Fundamental component}} - \overbrace{k_{reload} \cdot \frac{U_k}{U_d}}^{\text{3rd harmonic ref.}} + \frac{bias}{2} \tag{7.9a}$$

$$U_{L2_{compare}} = \frac{1}{\sqrt{3}} \cdot m_a \cdot k_{reload} \cdot \sin\left(2\pi \cdot f_1 \cdot t - 120^\circ\right) - k_{reload} \cdot \frac{U_k}{U_d} + \frac{bias}{2} \tag{7.9b}$$

$$U_{L3_{compare}} = \frac{1}{\sqrt{3}} \cdot m_a \cdot k_{reload} \cdot \sin\left(2\pi \cdot f_1 \cdot t + 120^\circ\right) - k_{reload} \cdot \frac{U_k}{U_d} + \frac{bias}{2} \tag{7.9c}$$

where

$$\begin{cases} m_a \leq 1.0, \\ U_k = \frac{1}{2} \cdot \left(\max\{U_{Ao1}, U_{Bo1}, U_{Co1}\} + \min\{U_{Ao1}, U_{Bo1}, U_{Co1}\}\right), \\ U_{Xo1} = \overbrace{m_a \cdot \frac{U_d}{\sqrt{3}}}^{\text{Eq. 2.15}} \cdot \sin\left(2\pi \cdot f_1 \cdot t + \theta_s\right), \\ bias = k_{reload} \end{cases}$$

How the third harmonic reference component from the expressions in Equation 7.9 is injected into the fundamental component of the sinusoidal control signal is illustrated in Figure 7.3. The triangular waveform shown in the figure corresponds to the amplitude that is subtracted from the fundamental component. Meanwhile, the sinusoidal waveform enveloping the triangular waveform is obtained from a Fast Fourier Transform (FFT) analysis of the triangular waveform. The outcome of the calculations results in the comparison values illustrated in the lower graph, depicting a full period at a frequency of 50 Hz.

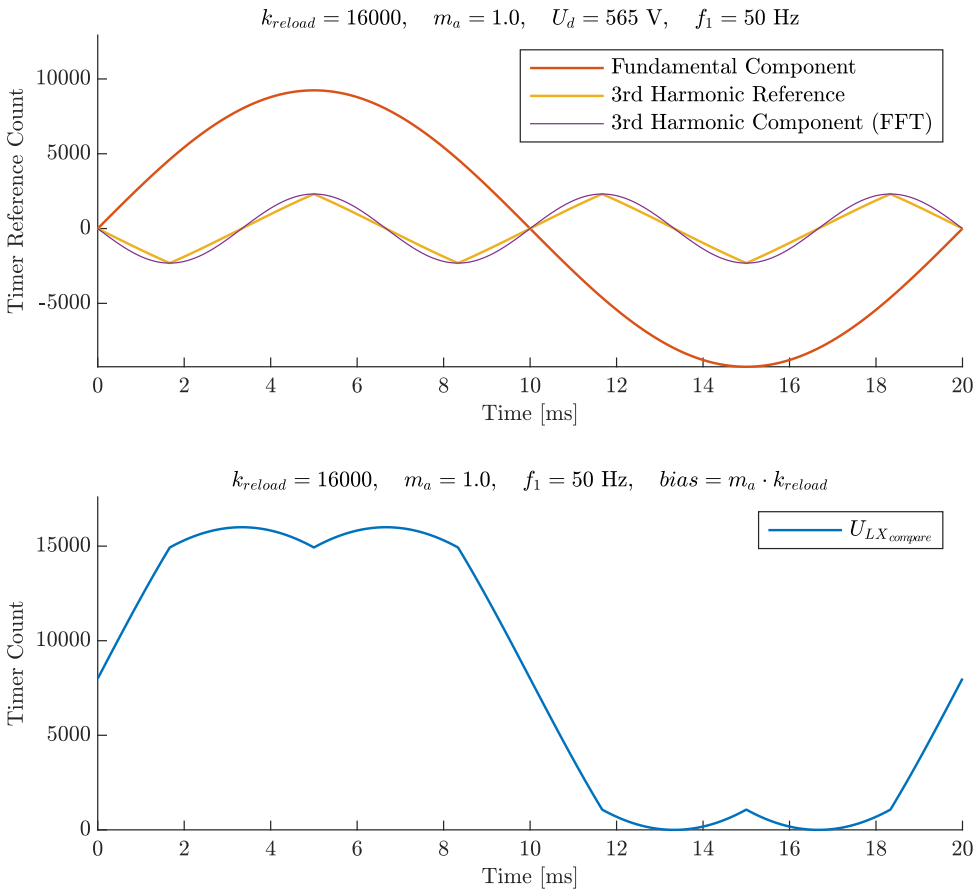


Figure 7.3: Injection of third harmonic content utilizing the SV-PWM algorithm.
Source: Created using MATLAB.

Under identical modulation conditions as depicted in Figure 7.2 ($m_a = 1.0$, $U_d = 565\,\text{V}_{\text{DC}}$, $f_1 = 50\,\text{Hz}$, and $f_s = 5\,\text{kHz}$), Figure 7.4 demonstrates the predicted voltage outcome when the inverter utilizes the SV-PWM algorithm for AC generation.

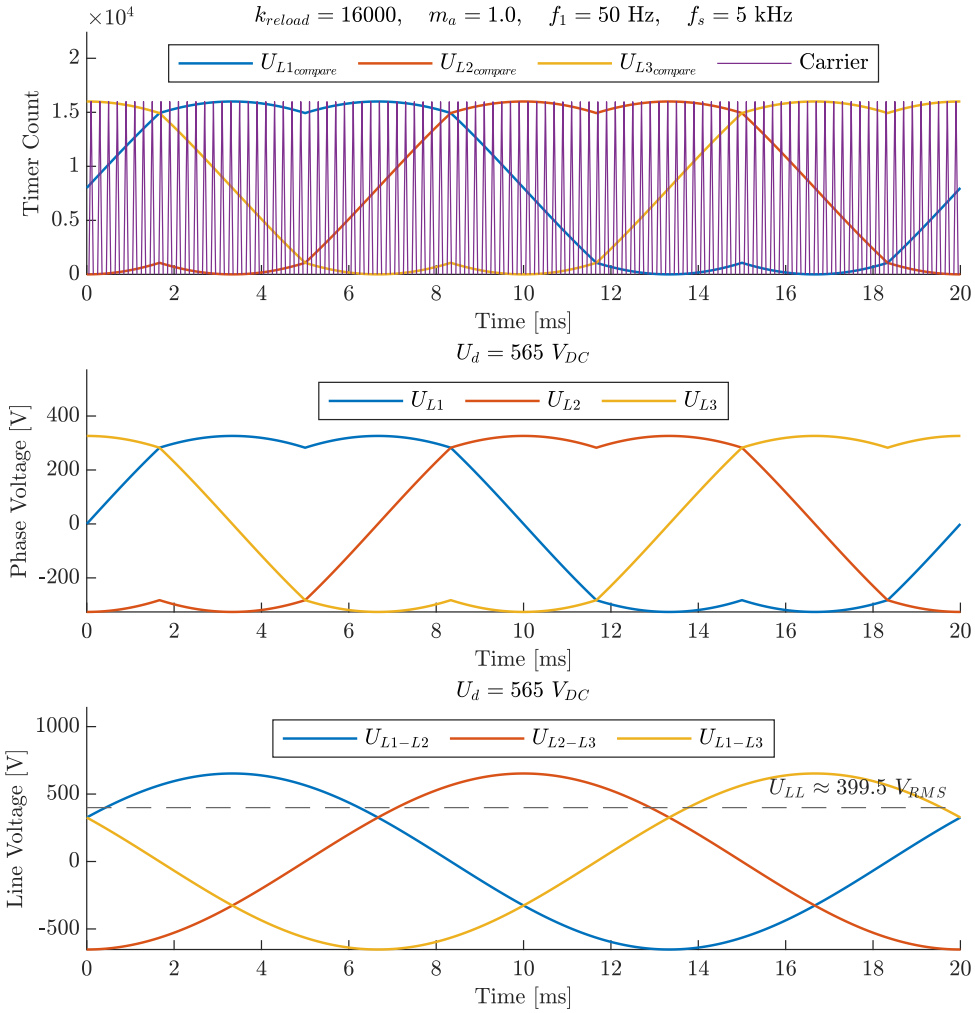


Figure 7.4: Anticipated outcome through the generation of a Space Vector PWM modulated signal ($U_d = 565\,\mathrm{V_{DC}}$).
Source: Created using MATLAB.

The comparative analysis of Figure 7.2 and Figure 7.4 reveals a noticeable enhancement in the output voltage of the inverter through the implementation of SV-PWM technique. The latter figure illustrates the space vector-based technique, which generates three phase voltages containing the same third harmonic component as the control signal, as discussed in Chapter 2.3. However, these third harmonic components are nullified in the line voltages, enabling the inverter to produce three sinusoidal line voltages of approximately $400\,\mathrm{V_{RMS}}$, as determined by Equation 2.17. This represents an approximate increase of 15 % compared to the maximum achievable output voltage through the SPWM approach, which was limited to generating line voltages of approximately $346\,\mathrm{V_{RMS}}$ utilizing the same DC-link voltage ($565\,\mathrm{V_{DC}}$).

Part III

Laboratory Experiments

Chapter 8

Laboratory Testing

To validate the efficacy of the inverter design in practical applications, it is essential to conduct laboratory experiments that scrutinize the design's response to diverse loads. The problem analysis detailed in Chapter 4.3 revealed that a resistive load and an inductive load, in the form of an induction motor, represent the minimal prerequisites for the test procedure. The testing methodology explicated in the present chapter aims to verify the design and compare the different algorithms implemented in the microcontroller. The outcomes of these tests are discussed in Chapter 9.

8.1 Elementary Function Tests

This section pertains to the foundational testing of the inverter, where the principal aim of the testing methodology is to verify the effectiveness of the design. This encompasses assessments of pulse width modulation generation, as well as more intricate tests to verify the proper functioning of all constituent sub-circuits.

Validation of PWM Signal Generation

Figure 8.1 presents the oscilloscope readings obtained during the evaluation of PWM generation by the microcontroller. The oscilloscope was directly interfaced with the microcontroller pins, which had been configured to generate PWM signals on two complementary pins, signifying high side and low side. The duty cycle was set at a fixed value of 50 %, and the switching frequency was 5 kHz, with zero dead-time between switching operations.

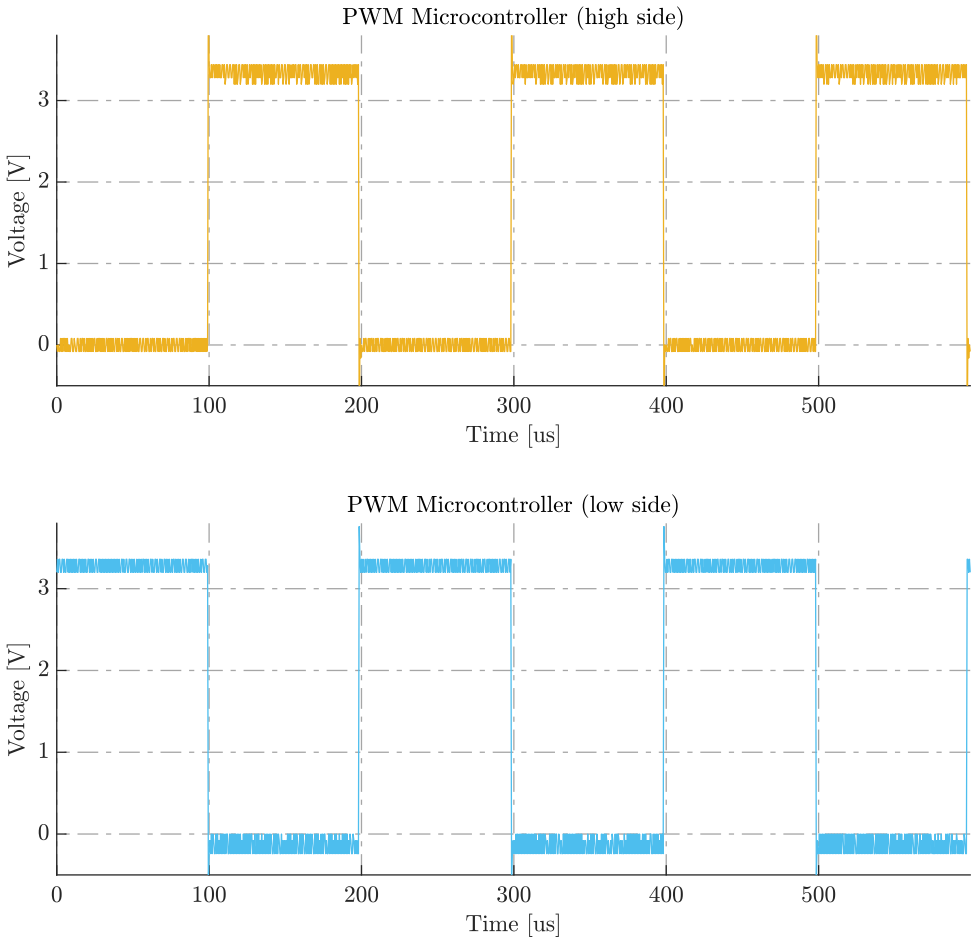
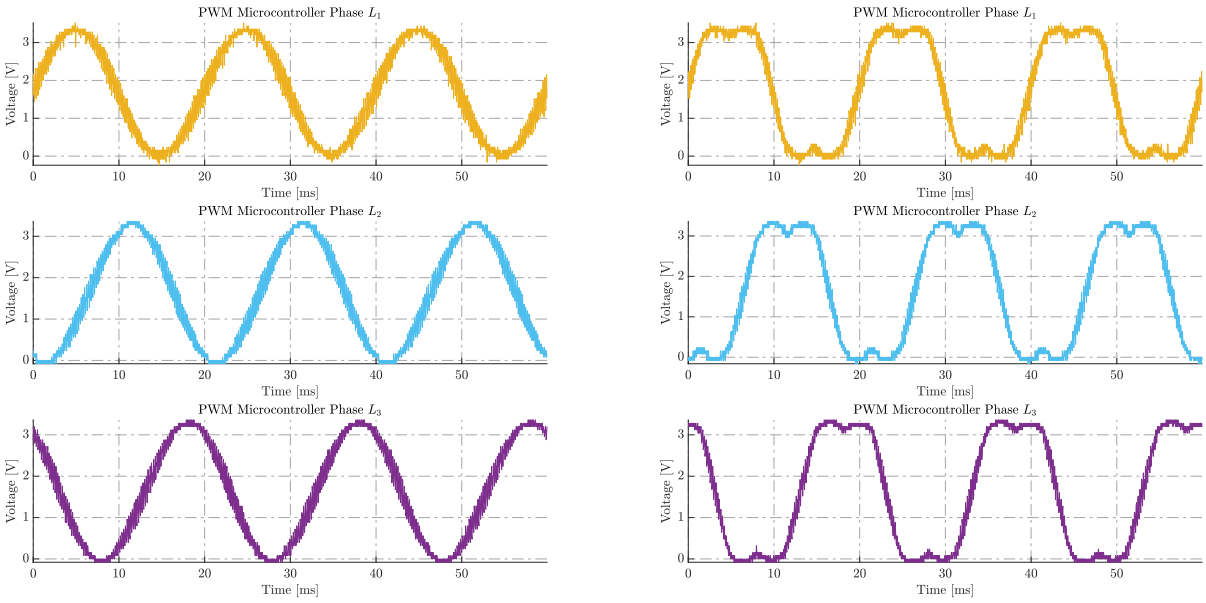


Figure 8.1: Validation of PWM signal generation ($D = 50\,\%$, $f_s = 5\,\text{kHz}$).
Source: Created using MATLAB (data from oscilloscope).

Likewise, Figure 8.2 showcases measurements akin to Figure 8.1, albeit with the microcontroller configured to generate three PWM signals utilizing the SPWM and SV-PWM technique, presented in Figures 8.2a and 8.2b, respectively. The amplitude modulation index was set to 1.0, and the measurements was filtered using a star-connected RC low-pass

filter[1] to suppress noise interference and facilitate the clear visualization of the sinusoidal waveforms on the oscilloscope.



(a) Results from SPWM generation.

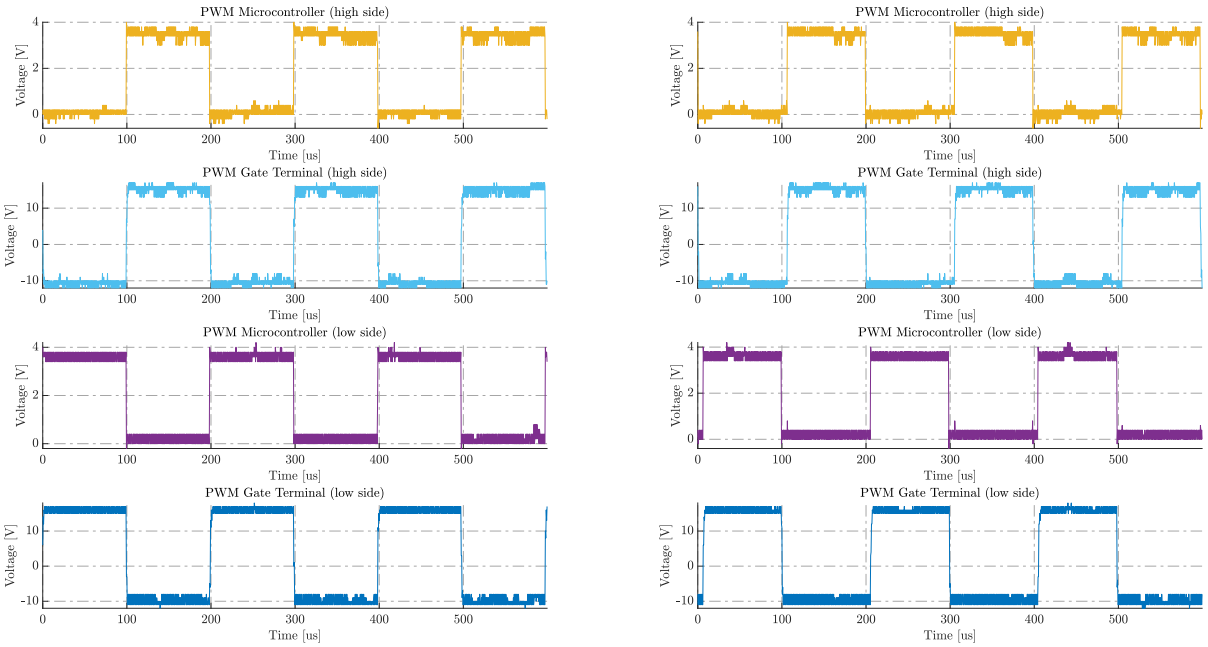
(b) Results from SV-PWM generation.

Figure 8.2: PWM signal generation utilizing the SPWM and SV-PWM technique ($m_a = 1.0$, $f_1 = 50\,\text{Hz}$, $f_s = 5\,\text{kHz}$).
Source: Created using MATLAB (data from oscilloscope).

Verification of Gate Driver Circuitry

Figure 8.3 depicts the measurement data collected from the oscilloscope that was connected to two complementary pins of the microcontroller, as well as the gate terminals of the high side and low side on a randomly selected leg of the inverter ($R_{gate} = 100\,\Omega$). Furthermore, the microcontroller was configured to generate PWM signals with a duty cycle of 50 % at a rate of 5 kHz. The results obtained without any dead-time from the microcontroller are shown in Figure 8.3a, while Figure 8.3b demonstrates the same measurements with a maximum possible dead-time. The test was conducted in the absence of any DC-link voltage.

[1] The low-pass filter was configured with $R \approx 2.74\,\text{k}\Omega$ and $C \approx 115.2\,\text{nF}$, implying a cut-off frequency of approximately 500 Hz.



(a) PWM signal generation without MCU dead-time.

(b) PWM signal generation with maximal MCU dead-time.

Figure 8.3: Comparison of PWM signals with and without dead-time from the microcontroller ($D = 50\,\%$, $f_s = 5\,\text{kHz}$, $U_d = 0\,\text{V}_\text{DC}$, $R_{gate} = 100\,\Omega$).
Source: Created using MATLAB (data from oscilloscope).

Controlling Switching Behavior

Figure 8.4 illustrates the measurements obtained from the oscilloscope during a test that involved connecting a single leg of the inverter to a DC-link voltage of $500\,\text{V}_\text{DC}$. The leg was connected to a resistive load of $144\,\Omega$ in parallel with the lower transistor[2], and both transistors were equipped with gate resistors of $100\,\Omega$. The microcontroller was configured to generate PWM signals with a duty cycle of $50\,\%$ at a switching frequency of $5\,\text{kHz}$. The test was conducted under the maximum dead-time setting from the microcontroller.

[2] In order to enable testing of the current sensor in Figure 8.5 at various levels of current, a resistance with high internal inductance has been deliberately selected.

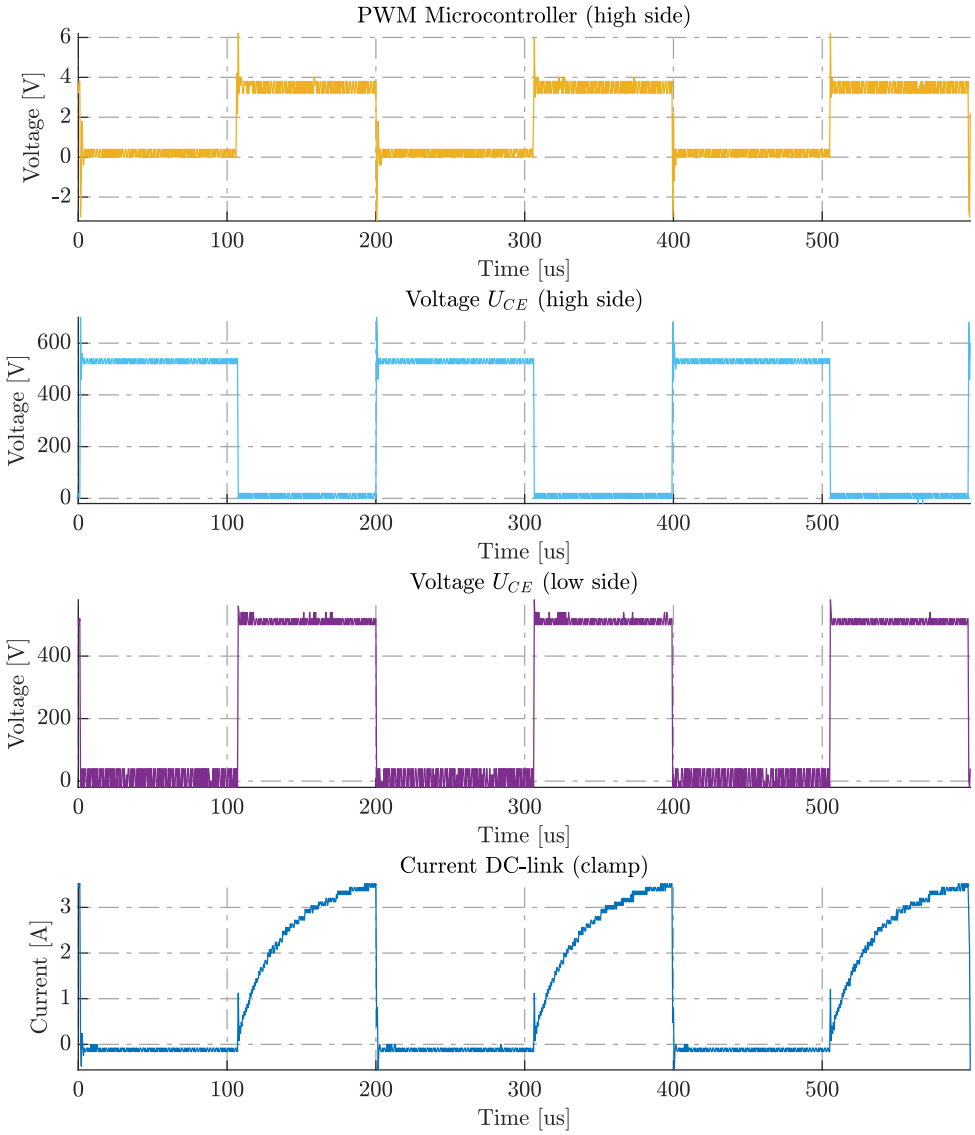


Figure 8.4: Switching behavior of the transistors ($D = 50\,\%$, $f_s = 5\,\mathrm{kHz}$, $U_d = 500\,\mathrm{V_{DC}}$, $R_{gate} = 100\,\Omega$).
Source: Created using MATLAB (data from oscilloscope).

Verification of Current Sensor Circuitry

The oscilloscope readings in Figure 8.5 are obtained from the same test as Figure 8.4. However, the emphasis is placed on extracting the analog output measurements from the internal current sensors of the inverter. The depicted figure also showcases the current measurements gathered through a current clamp, serving as a reference for comparative analysis. Additionally, this signal is compared to the expected output derived from the sensor's datasheet.

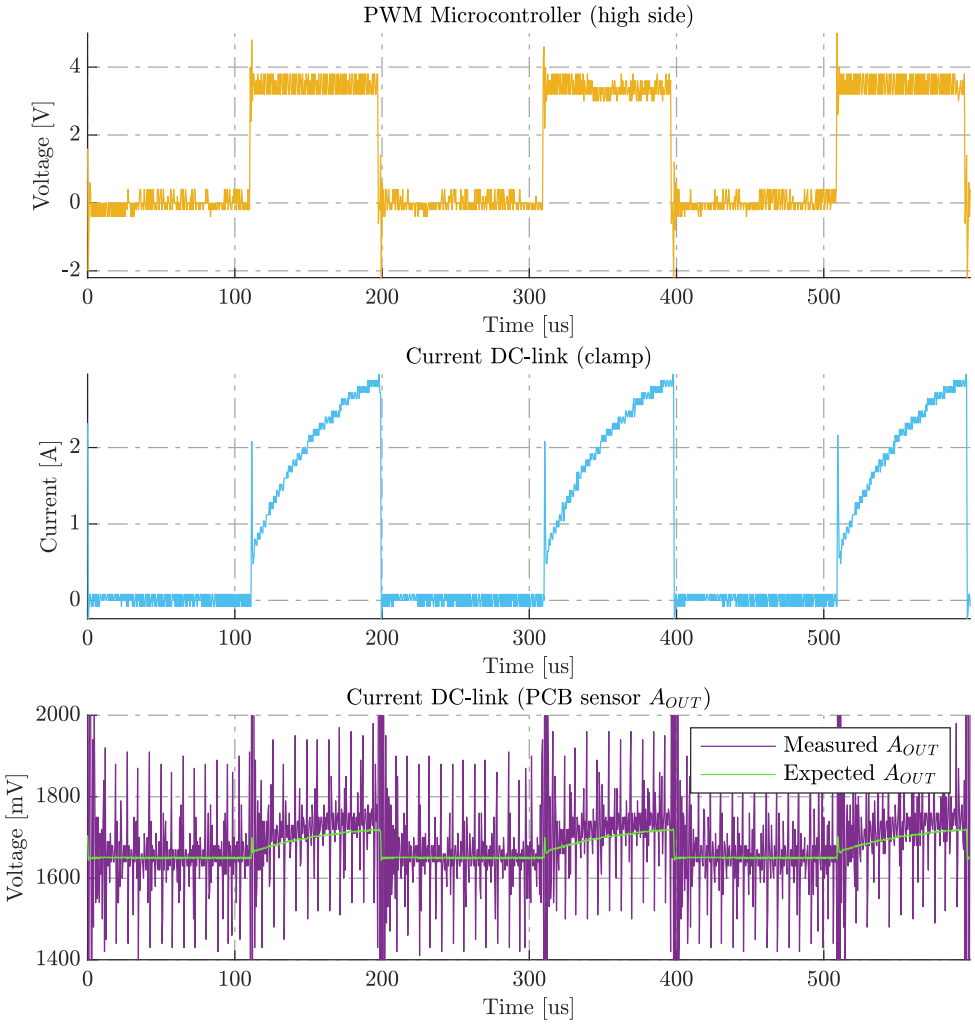
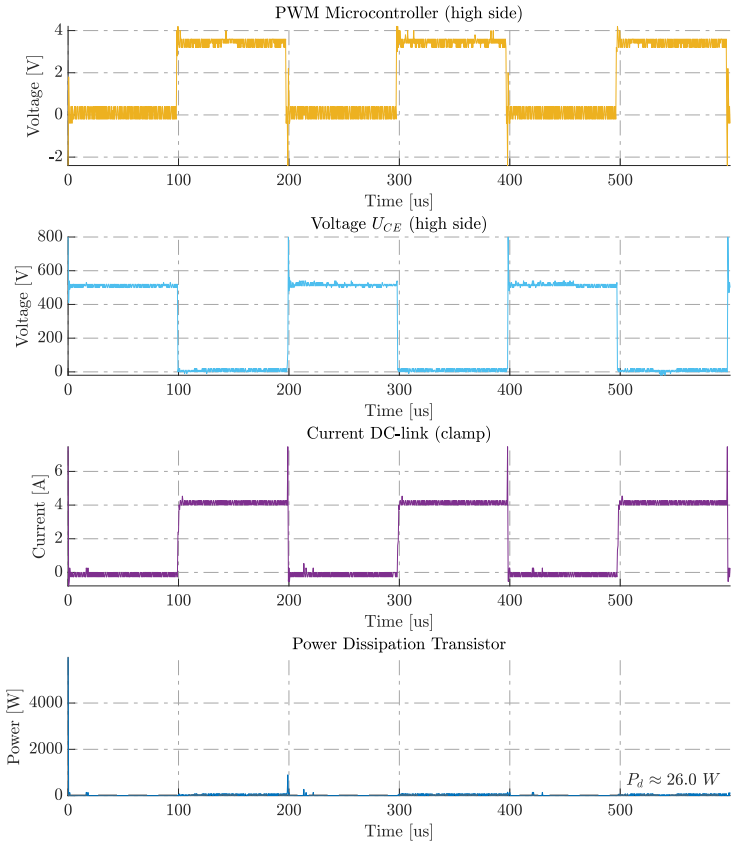


Figure 8.5: Verification of current sensor circuitry ($D = 50\,\%$, $f_s = 5\,\text{kHz}$, $U_d = 500\,\text{V}_\text{DC}$, $R_{gate} = 100\,\Omega$).
Source: Created using MATLAB (data from oscilloscope).

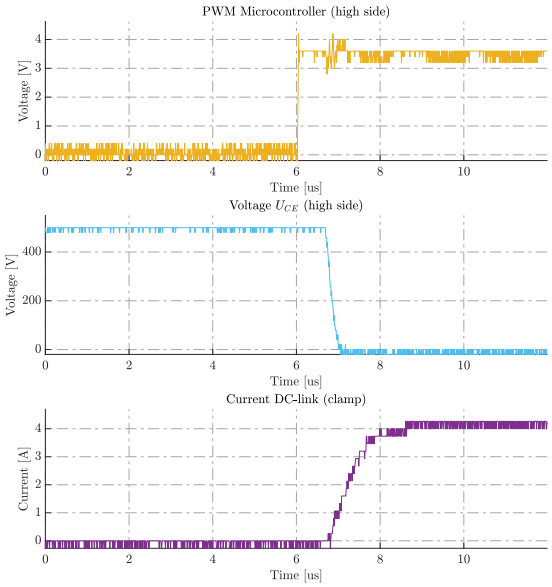
Effects of Different Gate Resistors

The measurement results presented in Figures 8.6, 8.7, 8.8, and 8.9 illustrate a series of oscilloscope readings that were conducted at varying values of R_{gate}, sorted in a descending order. The data presented is focused on observing the impact of these values on the rising and falling edges of the collector-emitter voltage, U_{CE}, as well as the average power loss, P_d, throughout the period. The physical setup of the experiments illustrated in Figures 8.4 and 8.5 was replicated, with the only difference being the load resistor, which was replaced with one featuring lower internal inductance and a resistance value of $124\,\Omega$. The DC-link voltage was also held the same at $500\,\text{V}_\text{DC}$, and the dead-time from the microcontroller

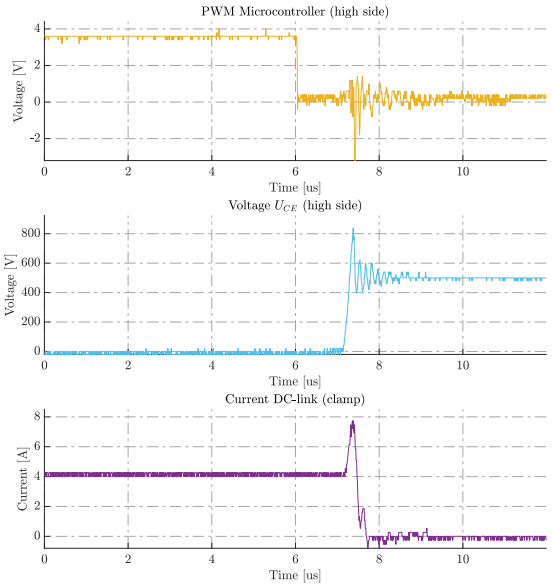
was lowered to 1/8 of the maximum possible value [22, p. 996].



(a) Power dissipation of transistor.

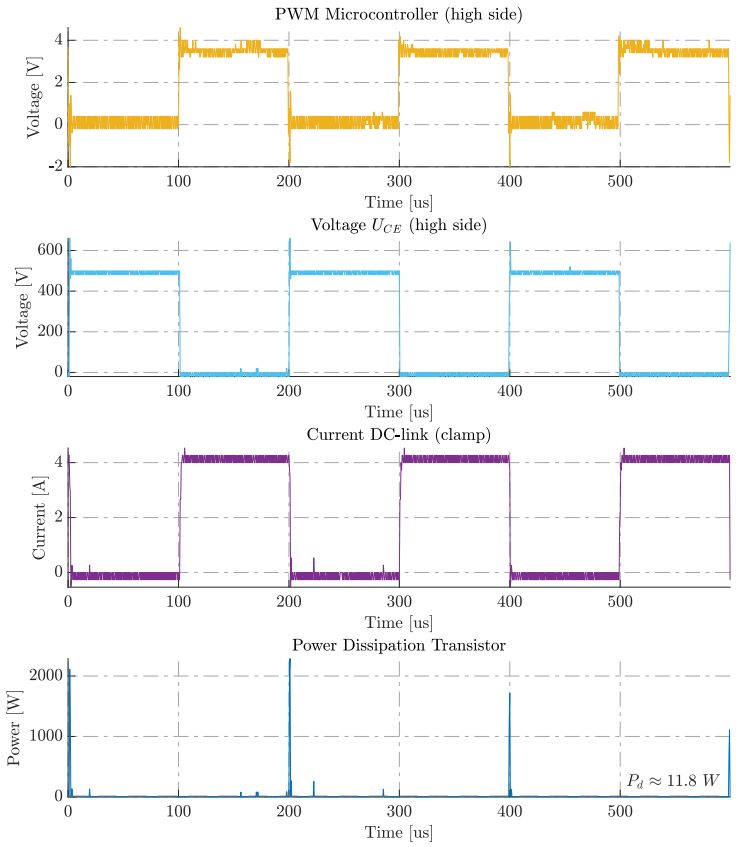


(b) Rising edge of the PWM signal.

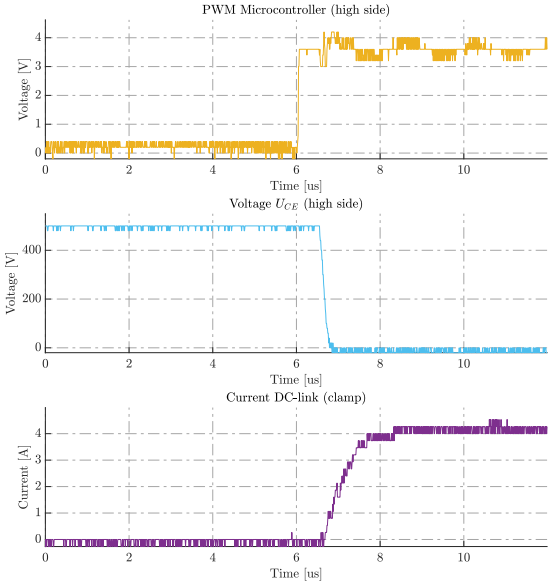


(c) Falling edge of the PWM signal.

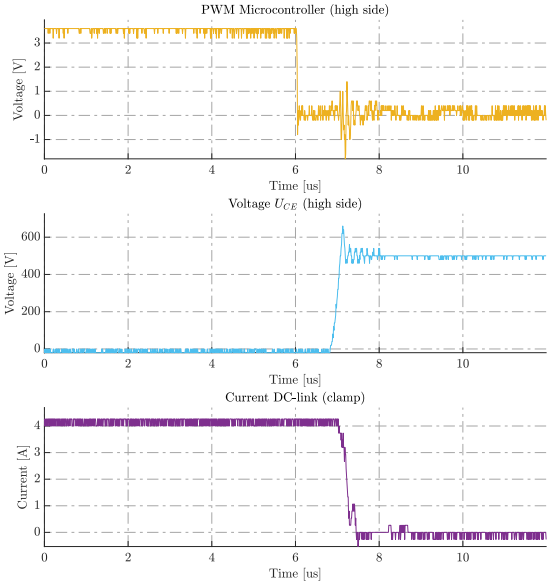
Figure 8.6: Comparison of the falling and rising edges of the collector-emitter voltage with $R_{gate} = 100\,\Omega$ ($D = 50\,\%$, $f_s = 5\,\mathrm{kHz}$, $U_d = 500\,\mathrm{V_{DC}}$).
Source: Created using MATLAB (data from oscilloscope).



(a) Power dissipation of transistor.

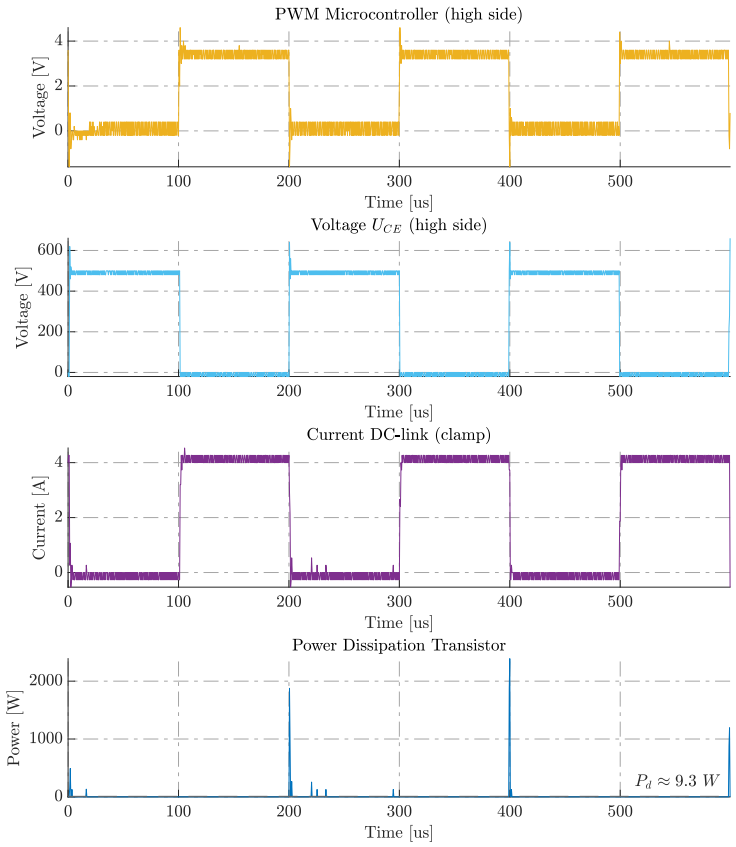


(b) Rising edge of the PWM signal.

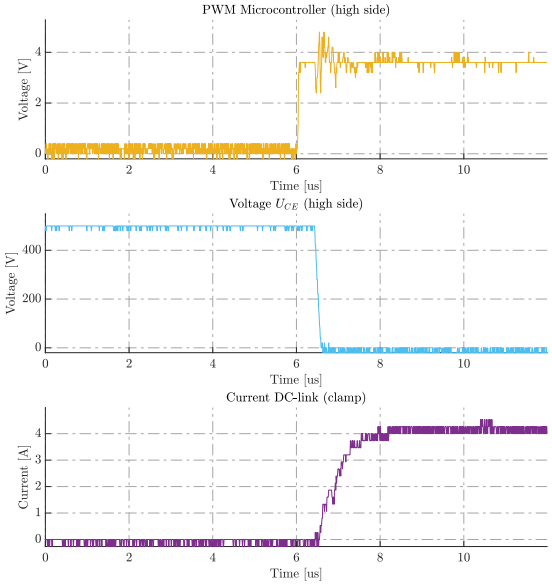


(c) Falling edge of the PWM signal.

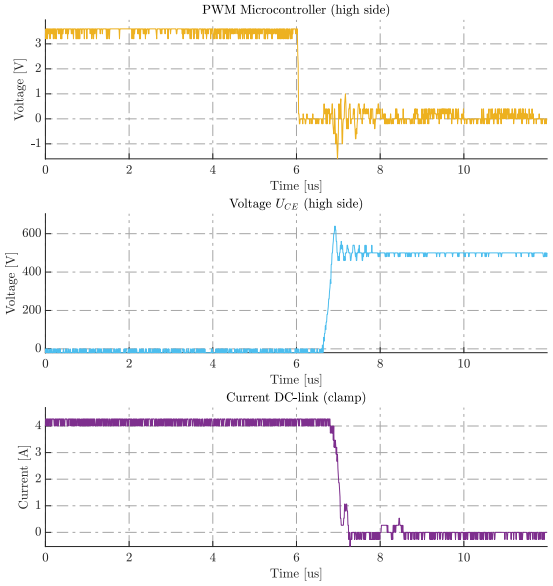
Figure 8.7: Comparison of the falling and rising edges of the collector-emitter voltage with $R_{gate} = 75\,\Omega$ ($D = 50\,\%$, $f_s = 5\,\text{kHz}$, $U_d = 500\,\text{V}_\text{DC}$).
Source: Created using MATLAB (data from oscilloscope).



(a) Power dissipation of transistor.

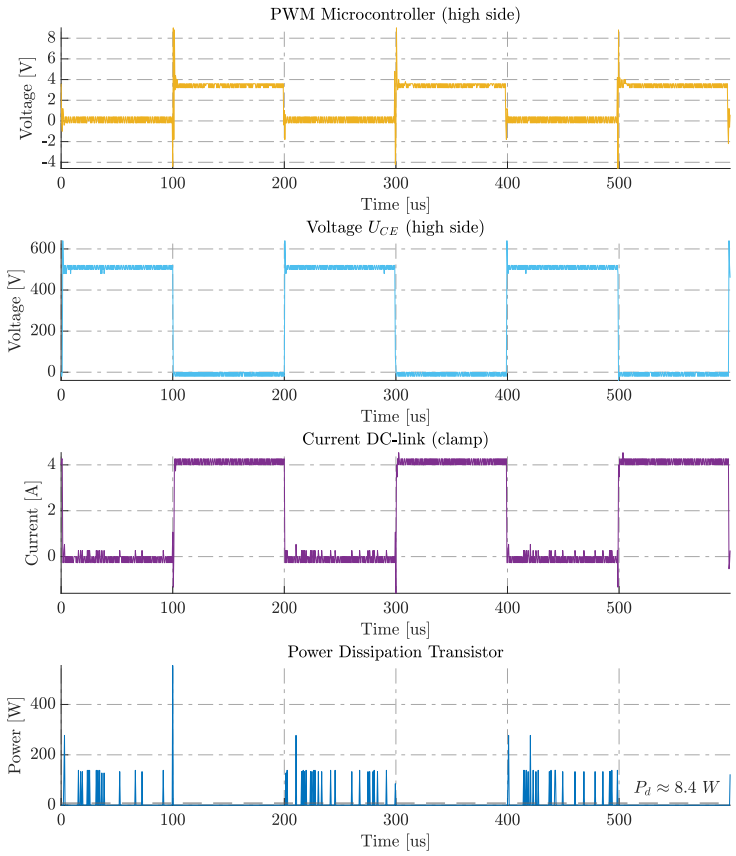


(b) Rising edge of the PWM signal.

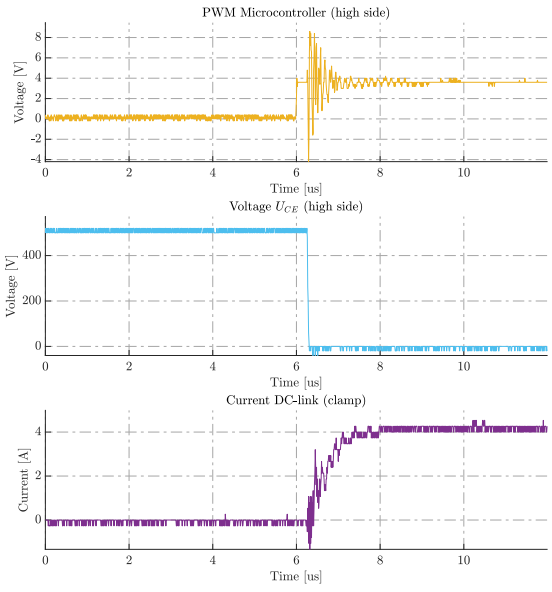


(c) Falling edge of the PWM signal.

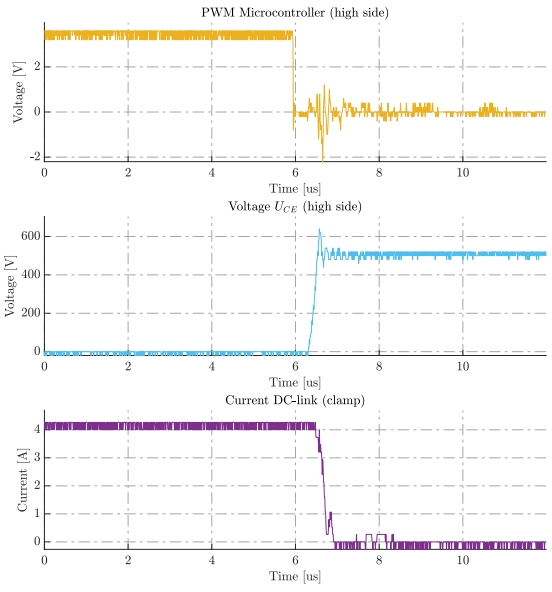
Figure 8.8: Comparison of the falling and rising edges of the collector-emitter voltage with $R_{gate} = 50\,\Omega$ ($D = 50\,\%$, $f_s = 5\,\text{kHz}$, $U_d = 500\,\text{V}_\text{DC}$).
Source: Created using MATLAB (data from oscilloscope).



(a) Power dissipation of transistor.



(b) Rising edge of the PWM signal.



(c) Falling edge of the PWM signal.

Figure 8.9: Comparison of the falling and rising edges of the collector-emitter voltage with $R_{gate} = 12\,\Omega$ ($D = 50\,\%$, $f_s = 5\,\mathrm{kHz}$, $U_d = 500\,\mathrm{V_{DC}}$).
Source: Created using MATLAB (data from oscilloscope).

8.2 Motor Operation Tests

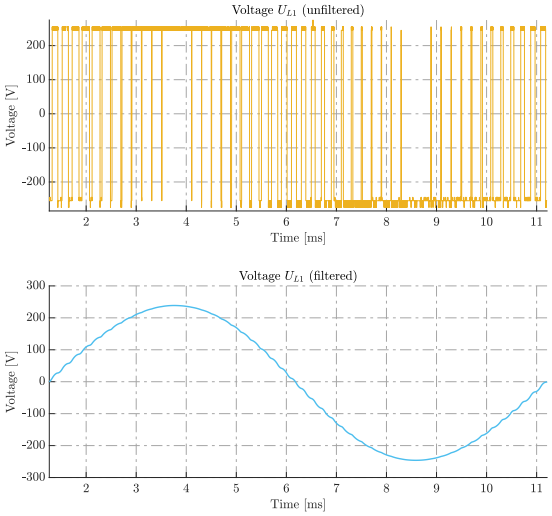
As discussed in Chapter 9.1, the results obtained from the elementary function tests carried out in Section 8.1 have enabled the circuit board to undergo further testing in accordance with its intended application, as it satisfies the fundamental requirements for basic operation. The ensuing tests are based on a three-phase load arrangement and endeavor to appraise the output voltages that can be attained through the diverse modulation algorithms when the inverter is connected to an induction motor[3][4].

Sinusoidal PWM Signal Generation

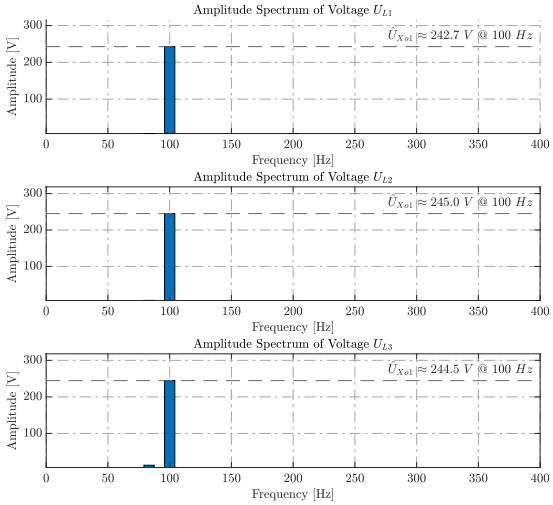
The oscilloscope measurements presented in Figure 8.10 are intended to serve as a benchmark for evaluating the corresponding theory laid out in Chapter 2.2. Specifically, the inverter was configured to generate a three-phase AC voltage using the Sinusoidal Pulse Width Modulation technique with an amplitude modulation index, m_a, of 1.0. The test was conducted under nominal operating conditions as defined in Table 3.1, with the exception of the DC-link voltage, which was limited to $500\,\mathrm{V_{DC}}$ due to the unavailability of a rectifier with an output voltage of $565\,\mathrm{V_{DC}}$ that features built-in current limiting safety functions at the time of testing.

Figure 8.10a depicts the measurements of a phase voltage measured between a phase and the neutral point of the inverter, situated between two DC-link capacitors, as illustrated in Figure 2.1. The top plot displays the PWM of the output voltage, while the bottom plot portrays the same signal following filtration with a low-pass filter[5][6]. Furthermore, Figure 8.10b illustrates the Fast Fourier Transform (FFT) of the filtered voltage shown in Figure 8.10a, showcasing the three most prominent harmonic frequency components. Lastly, Figures 8.10c and 8.10d exhibit the three output phase and line voltages, respectively, along with the DC-link current measured using a current clamp.

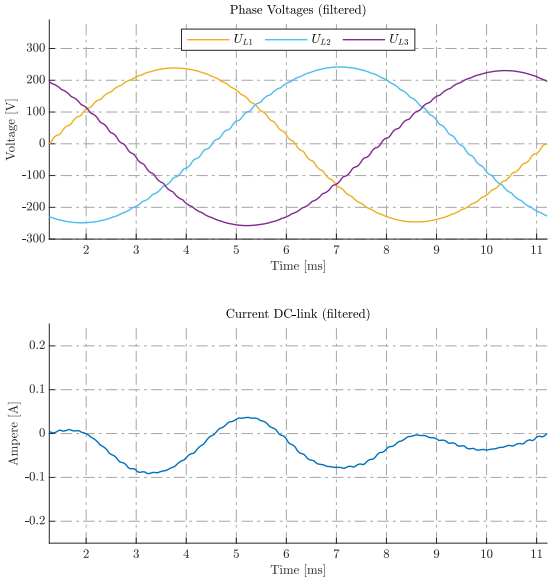
[3] The induction motor was not subjected to any mechanical load.
[4] The particular induction motor is specified in Appendix E.2.
[5] MATLAB was utilized to digitally filter the measurement data with a cut-off frequency of 500 Hz.
[6] The measurement data was generated at a sampling frequency of 5 MHz.



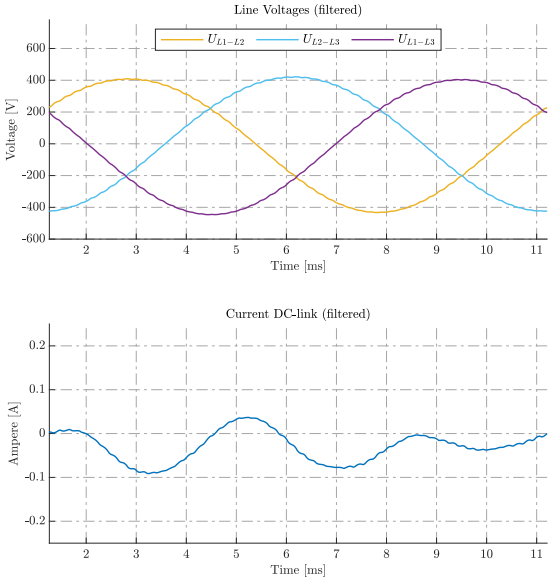
(a) Unfiltered and filtered phase voltage.



(b) FFT of filtered phase voltages.



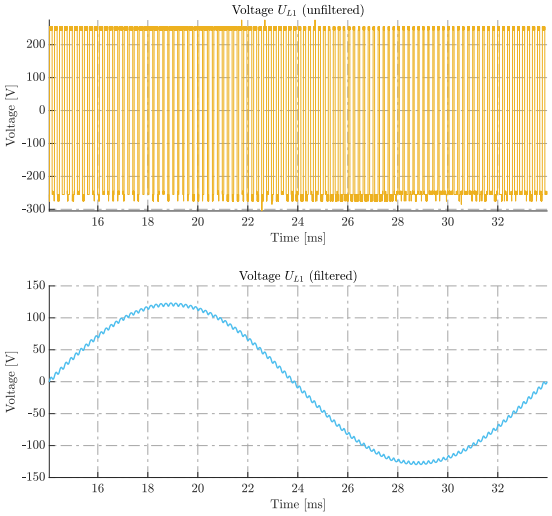
(c) Filtered phase voltages and DC current.



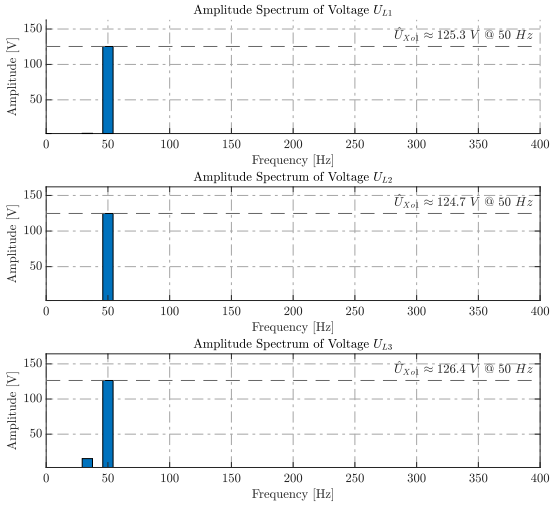
(d) Filtered line voltages and DC current.

Figure 8.10: Verified voltage outcome through the generation of a Sinusoidal PWM modulated signal ($R_{gate} = 50\,\Omega$, $f_1 = 100\,\text{Hz}$, $f_s = 5\,\text{kHz}$, $U_d = 500\,\text{V}_\text{DC}$, $m_a = 1.0$).
Source: Created using MATLAB (data from oscilloscope).

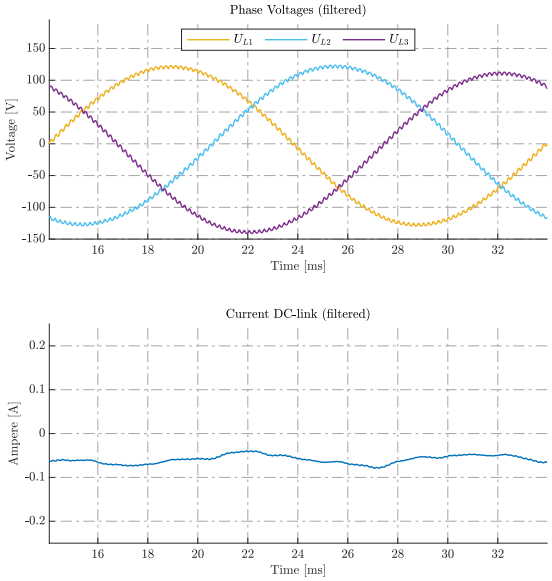
To confirm the inverter's ability to adjust the speed of the connected induction machine, tests were also conducted using different voltage and frequency settings. The measurements presented in Figure 8.11 were taken under the same conditions as those in Figure 8.10, but with a 50 % reduction in the output voltage and frequency, implying an amplitude modulation index $m_a = 0.5$ and a modulation frequency $f_1 = 50\,\text{Hz}$.



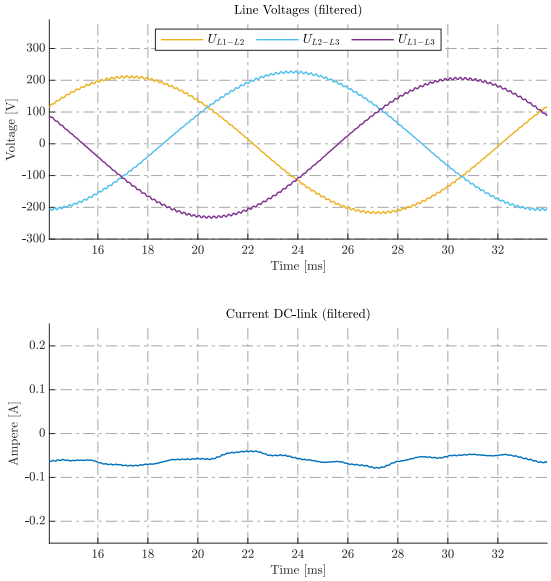
(a) Unfiltered and filtered phase voltage.



(b) FFT of filtered phase voltages.



(c) Filtered phase voltages and DC current.



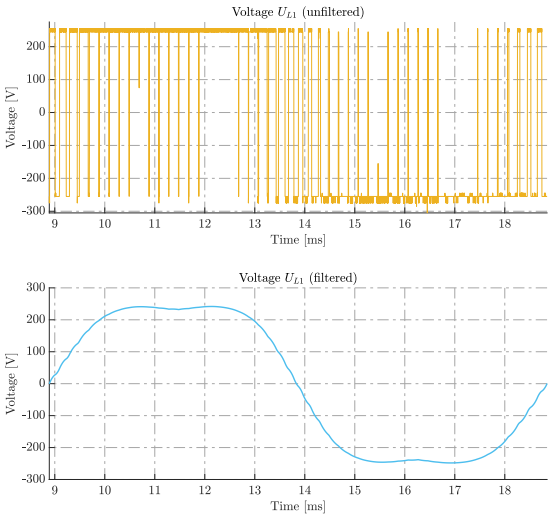
(d) Filtered line voltages and DC current.

Figure 8.11: Verified voltage outcome of a Sinusoidal PWM modulated signal with 50 % reduction in the $^{U}/_{f}$ ratio ($R_{gate} = 50\,\Omega$, $f_1 = 50\,\text{Hz}$, $f_s = 5\,\text{kHz}$, $U_d = 500\,\text{V}_\text{DC}$, $m_a = 0.5$).
Source: Created using MATLAB (data from oscilloscope).

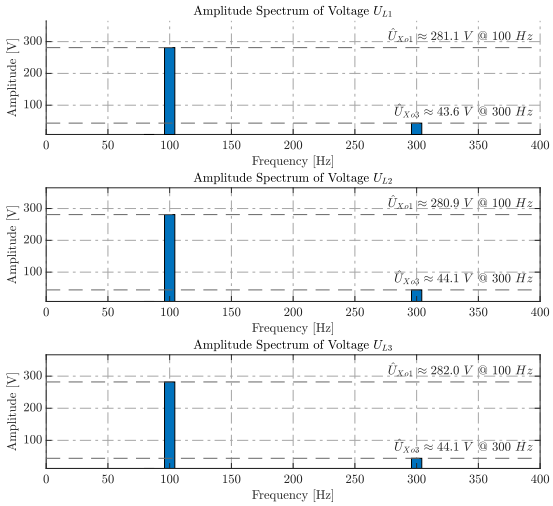
Space Vector PWM Signal Generation

Similar to the preceding section pertaining to the generation of SPWM signals, this subsequent set of measurement outcomes portrays oscilloscope readings obtained through the utilization of the Space Vector Pulse Width Modulation technique. Specifically, Figure 8.12 corresponds to the SPWM approach depicted in Figure 8.10. Similarly,

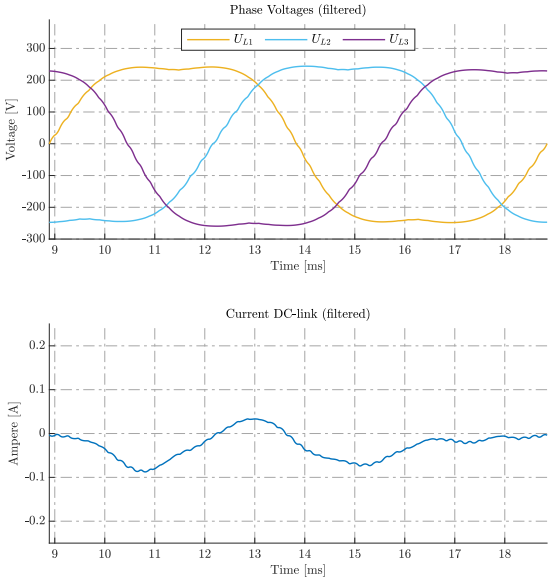
Figure 8.13 is comparable to Figure 8.11.



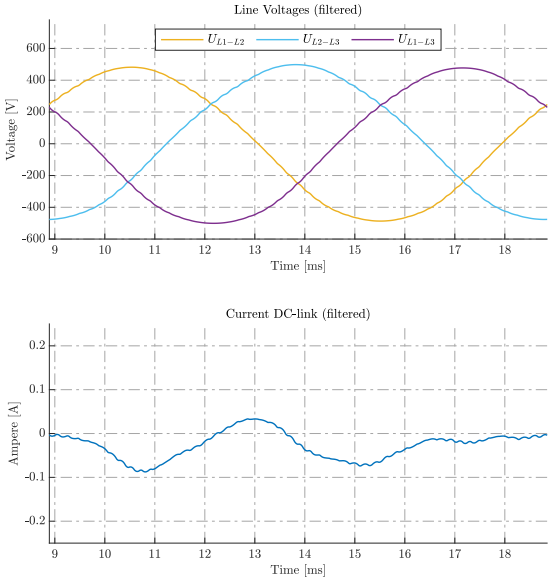
(a) Unfiltered and filtered phase voltage.



(b) FFT of filtered phase voltages.

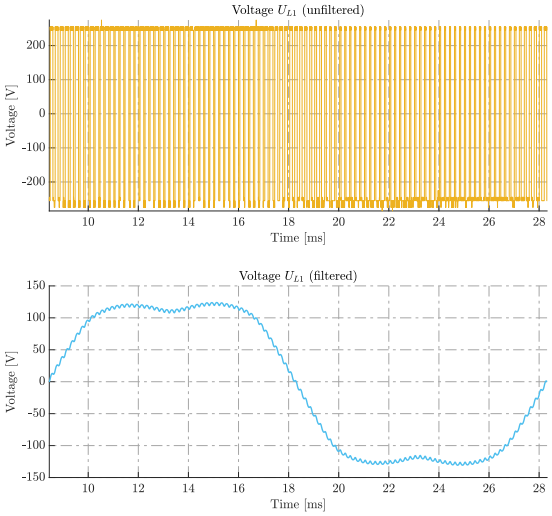


(c) Filtered phase voltages and DC current.

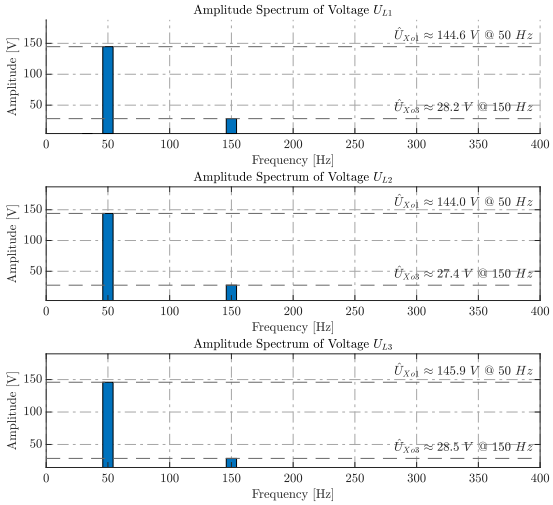


(d) Filtered line voltages and DC current.

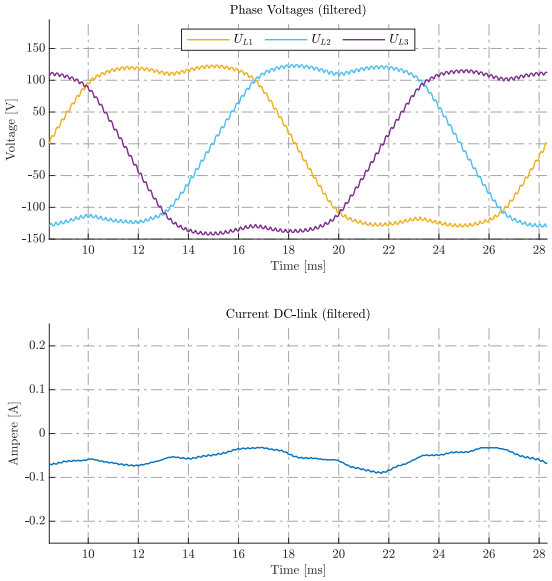
Figure 8.12: Verified voltage outcome through the generation of a Space Vector PWM modulated signal ($R_{gate} = 50\,\Omega$, $f_1 = 100\,\text{Hz}$, $f_s = 5\,\text{kHz}$, $U_d = 500\,\text{V}_\text{DC}$, $m_a = 1.0$).
Source: Created using MATLAB (data from oscilloscope).



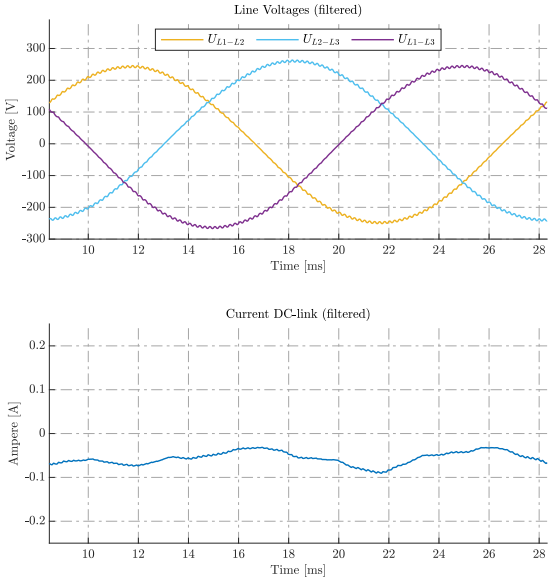
(a) Unfiltered and filtered phase voltage.



(b) FFT of filtered phase voltages.



(c) Filtered phase voltages and DC current.



(d) Filtered line voltages and DC current.

Figure 8.13: Verified voltage outcome of a Space Vector PWM modulated signal with 50 % reduction in the $^{U}/_{f}$ ratio ($R_{gate} = 50\,\Omega$, $f_1 = 50\,\text{Hz}$, $f_s = 5\,\text{kHz}$, $U_d = 500\,\text{V}_\text{DC}$, $m_a = 0.5$).
Source: Created using MATLAB (data from oscilloscope).

Chapter 9

Results Analysis

This chapter presents an analysis of the laboratory experiments carried out in Chapter 8, with the objective of assessing the efficiency of the inverter developed in the present project. The chapter is divided into discrete sections, each corresponding to key topics that are essential to verify the design. It furnishes a comprehensive evaluation of the inverter's effectiveness, proffering valuable insights into its strengths, limitations, and potential avenues for future enhancement.

9.1 Discussion of Fundamental Tests

To assess the inverter's suitability for further testing with three-phase loads, the present section endeavors to discuss the tests conducted in Chapter 8.1. This evaluation assumes critical importance, as the tests undertaken pertain to the inverter's ability in executing fundamental operations such as generating PWM (Pulse Width Modulation) signals, as well as verifying its sub-circuits.

Gate Driver Circuitry

In conclusion, the gate driver circuitry has proven to effectively control the IGBTs (Insulated-Gate Bipolar Transistors), demonstrating successful operation. Its accurate switching signals have enabled precise control over the IGBTs' conduction and blocking states. Figure 8.3 provides clear evidence that the control signal, generated by the microcontroller, successfully reaches gate of both the low-side and the high-side IGBT, with inverted control signals. Additionally the data unequivocally verifies that the gate of the IGBT receives the appropriate control voltage from the isolated DC-DC converters, measuring a peak value of 15 V and a minimum value of −8 V.

Figure 8.4 presents conclusive evidence that the gate control signal effectively triggered the blocking and conduction states of the IGBT, facilitating current flow. When the high-side IGBT was activated, the voltage drop across it rapidly decreased from the supplied DC-link voltage to approximately 0 V, while the voltage drop across the low-side IGBT concurrently rose from approximately 0 V to the provided DC-link voltage. Consequently, current circulated within the test circuit, validating the successful operation of the system.

Notwithstanding the presence of IGBT switching during the conducted tests employing a gate resistor of 100 Ω, it is imperative to acknowledge that the choice of gate resistor value significantly influences the switching characteristics of the IGBT, as elaborated upon in Section 9.2.

Current and Voltage Sensor Circuitry

During the analysis of the collected data, as depicted in Figure 8.5, significant disparities were observed between the anticipated and the measured output values. The measured voltage exhibited pronounced noise levels, which adversely impacted the precision of the measurements. This excessive noise presented considerable challenges in obtaining accurate readings, especially when employing an oscilloscope in the millivolt range. The presence of such heightened noise levels introduced uncertainties, obscuring the underlying signal amidst the interference. While the measured signal displayed waveform similarity to the

expected signal, a notable discrepancy arose when attempting to precisely capture the signal for microcontroller-based current calculations in the circuit. Enhancements to the implemented filter on Aout, as found in B.10, could effectively reduce the undesired noise.

The measurement of the DC-link voltage has not been fully tested due to the absence of an operational amplifier. However, primary tests have been conducted to confirm the accuracy of the voltage divider circuit, as well as the proper functioning and voltage output of the isolation amplifier. Specifically, 0 V DC-link voltage results in a 0 V output from the isolation amplifier, while a 500 V DC-link voltage yields a 1 V output from the amplifier. The results were obtained using a multimeter. However, no testing has been performed beyond the isolation amplifier and onward to the operational amplifier, presented in detail in Appendix B.11.

9.2 Impact of Varying Gate Resistors

Gate resistors have a significant influence on the switching performance of transistors, affecting parameters such as rise time and peak values of currents and voltages. As expounded in Chapter 6, this affects the determination of power dissipation in the semiconductors, which ultimately dissipates as heat. The following section provides a detailed discussion of how these factors were influenced in the laboratory experiments conducted in Chapter 8.1.

Power Dissipation

As seen in Figures 8.6a, 8.7a, 8.8a and 8.9a it is clear that power dissipation of the transistors, P_d, descends as a lower value for gate resistance, R_{gate}, is utilized. Based on the conducted measurements, a power dissipation of 26 W has been measured at 100 Ω gate resistance and 8.24 W at 12 Ω, the same correlation in verified in Appendices D.5, D.6, D.7 and D.8 thus with reduced levels of noise compared to the measurements obtained in Figures 8.6a, 8.7a, 8.8a and 8.9a. The observed data from the figures suggests that the presence of noise in current measurements can significantly influence power dissipation,

as it is obtained by multiplying voltage and current measurements. The contrasting levels of noise in voltage and current measurements may account for the discrepancy observed between the simulated and measured values of power dissipation. The switching loss moments are captured in Figures 8.6b, 8.6c, 8.7b, 8.7c, 8.8b, 8.8c, 8.9b and 8.9c. They show a harder switching as R_{gate} descends, resulting in less loss from the switching moments.

As of the estimated power dissipation in Equation 6.10 from Chapter 6.1 there is a correlation, but with discrepancy. Possible reasons for these discrepancies may entail a change in duty cycle during measurements due to dead time as mentioned in Chapter 8.1, resulting in a slightly reduced duty cycle and thereby a smaller loss. Other reasons for the discrepancies may include the noise from the current measurement, as previously mentioned. Another possible reason for the discrepancy could be inaccuracies in the parameters utilized during the calculations. This discrepancy may arise because certain values had to be estimated from various graphs within the datasheet, introducing a level of uncertainty into the calculations. It is essential to acknowledge that both simulations and calculations are approximations, and there is typically a disparity between the measured values and the simulated or calculated results. Insufficient precision in the measurements obtained prevents conclusive statements regarding the actual power dissipation, primarily due to the presence of significant noise in the measurements.

Switching Response

The switching response of an IGBT is influenced by the value of the gate resistor, as substantiates by data in Figures 8.6b, 8.6c, 8.7b, 8.7c, 8.8b, 8.8c, 8.9b and 8.9c. Variations in the gate resistor value significantly impact the switching characteristics of the IGBT. With $R_{gate} = 12\,\Omega$, the switching speed of the IGBT was notably faster, resulting in a shorter rise and fall time compared to higher gate resistor values. However, the increase speed also led to a faster peak current during switching transitions.

On the other hand, employing $R_{gate} = 100\,\Omega$ slowed down the switching speed, resulting in longer rise and fall times, and slower peak currents. At the same time, voltage spikes

of nearly 800 V occurred when switching off the IGBT, compared to 600 V with a 12 Ω gate resistor. Intermediate values, $R_{gate} = 50\,\Omega$ and $R_{gate} = 75\,\Omega$ offered a compromise between switching speed and peak voltage and current. These observations emphasize the importance of carefully selecting the appropriate gate resistor to achieve the desired trade-off between switching speed and current handling capabilities in IGBT applications.

For subsequent testing, $R_{gate} = 50\,\Omega$ was selected to ensure a conservative approach and avoid subjecting the IGBTs to excessive stress during switching operations. It is important to acknowledge that the chosen gate resistor value is not fully optimized and should be further tailored to the specific requirements of the final inverter design. Fine-tuning the gate resistor value based on comprehensive analysis and performance considerations will be crucial to achieve optimal operation and efficiency in the inverter.

9.3 Comparison of Modulation Algorithms

As discussed in theoretical chapters 2.2 and 2.3, regarding Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SV-PWM) respectively, the latter modulation algorithm aims to utilize the available DC-link voltage more effectively than the former. In nominal operation of the inverter, it was expected to generate line voltages with RMS values of approximately $346\,V_{RMS}$ and $400\,V_{RMS}$, as illustrated in Figures 7.2 and 7.4 for SPWM and SV-PWM, respectively.

This section aims to confirm whether the underlying theory holds true or not, where a summary of the measurements conducted in Chapter 8.2 and the theoretical foundation outlined in Chapter 2 has been compiled in Table 9.1. The measurements can be directly compared with Figures 8.10 and 8.12 from the laboratory experiments.

Measurement Value[1,2]		SPWM		SV-PWM	
		Calc.	**Measured**	**Calc.**	**Measured**
Output Phase Voltage L_1	$\hat{U}_{L1_1}$	250.0 V	242.7 V	288.7 V	281.1 V
	$\hat{U}_{L1_3}$	0 V	0 V	*ND*[3]	43.6 V
	$U_{L1_{RMS}}$	176.8 V	172.0 V	*ND*[3]	201.5 V
Output Phase Voltage L_2	$\hat{U}_{L2_1}$	250.0 V	245.0 V	288.7 V	280.9 V
	$\hat{U}_{L2_3}$	0 V	0 V	*ND*[3]	44.1 V
	$U_{L2_{RMS}}$	176.8 V	173.6 V	*ND*[3]	201.5 V
Output Phase Voltage L_3	$\hat{U}_{L3_1}$	250.0 V	244.5 V	288.7 V	282.0 V
	$\hat{U}_{L3_3}$	0 V	0 V	*ND*[3]	44.1 V
	$U_{L3_{RMS}}$	176.8 V	173.6 V	*ND*[3]	202.6 V
Output Line Voltage L_1-L_2	$\hat{U}_{L1-L2_1}$	433.0 V	418.8 V	500.0 V	485.0 V
	$\hat{U}_{L1-L2_3}$	0 V	0 V	0 V	0 V
	$U_{L1-L2_{RMS}}$	306.2 V	296.5 V	353.6 V	343.5 V
Output Line Voltage L_2-L_3	$\hat{U}_{L2-L3_1}$	433.0 V	422.5 V	500.0 V	487.4 V
	$\hat{U}_{L2-L3_3}$	0 V	0 V	0 V	0 V
	$U_{L2-L3_{RMS}}$	306.2 V	299.4 V	353.6 V	345.3 V
Output Line Voltage L_1-L_3	$\hat{U}_{L1-L3_1}$	433.0 V	426.7 V	500.0 V	489.4 V
	$\hat{U}_{L1-L3_3}$	0 V	0 V	0 V	0 V
	$U_{L1-L3_{RMS}}$	306.2 V	302.3 V	353.6 V	346.7 V

Table 9.1: Theoretical calculations versus oscilloscope readings ($U_d = 500\,\mathrm{V_{DC}}$, $m_a = 1.0$, $f_1 = 100\,\mathrm{Hz}$).

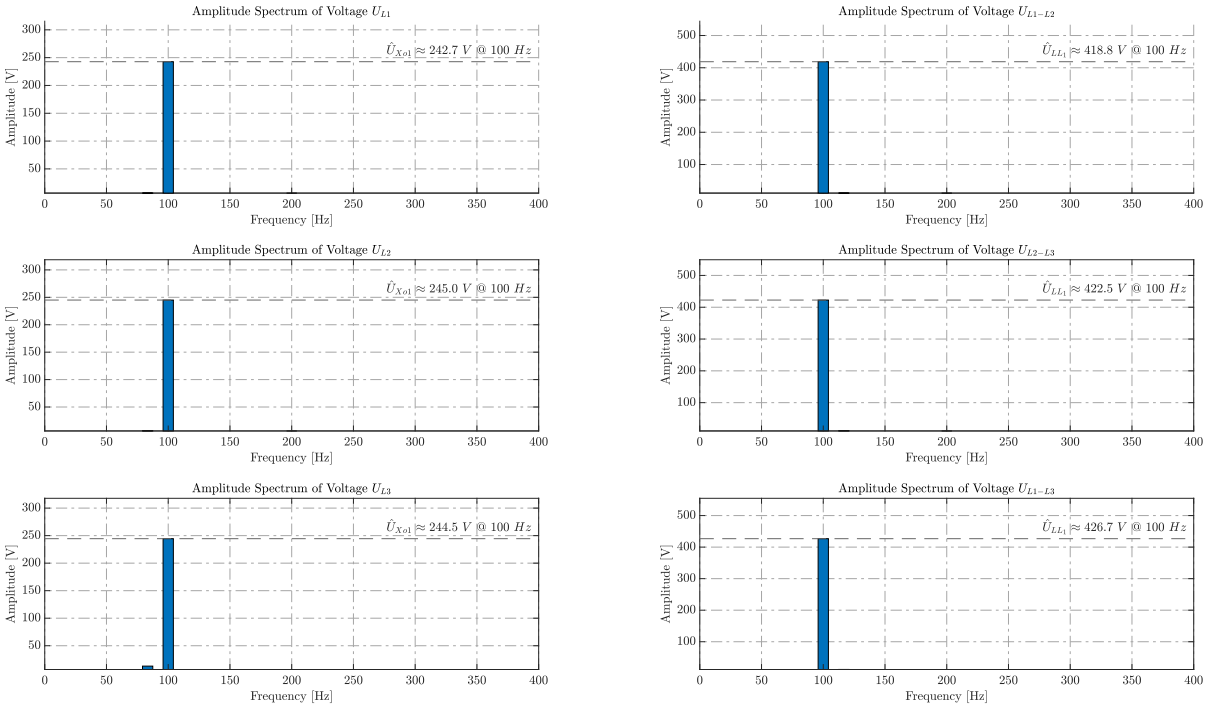
Figures 8.10 and 8.11 from the laboratory experiments exhibit measurements conducted on the inverter while employing the SPWM algorithm with a DC-link voltage of $500\,\mathrm{V_{DC}}$. According to Equation 2.9, when considering an amplitude modulation index of 1.0, the expected amplitude of the generated fundamental phase voltage should approximate

[1] The measured peak values have been calculated using the FFT function provided by MATLAB.
[2] The measured RMS values have been calculated using the RMS function provided by MATLAB.
[3] This report has omitted the explicit coverage of the theoretical framework pertaining to the determination of the amplitude of the third harmonic phase voltage in the context of SV-PWM.

250.0 V. This assertion is confirmed in practice by Figure 8.10b, wherein the Fast Fourier Transform (FFT) of the output phase voltages yields calculated fundamental amplitudes of $\hat{U}_{L1_1} = 242.7\,\mathrm{V}$, $\hat{U}_{L2_1} = 245.0\,\mathrm{V}$ and $\hat{U}_{L3_1} = 244.5\,\mathrm{V}$, accompanied by a fundamental frequency of $f_1 = 100\,\mathrm{Hz}$. Examining the figure, which is plotted for the three largest harmonic frequency components during the period, it is apparent that there are no other significant components, implying output phase voltages with low harmonic content.

Correspondingly, as per the theory, when the amplitude modulation index is set to 0.5, the expected output phase voltage peak is 125.0 V. This theoretical prediction is further substantiated by the measurements illustrated in Figure 8.11b, which showcases fundamental amplitudes of $\hat{U}_{L1_1} = 125.3\,\mathrm{V}$, $\hat{U}_{L2_1} = 124.7\,\mathrm{V}$ and $\hat{U}_{L3_1} = 126.4\,\mathrm{V}$, accompanied by a fundamental frequency of 50 Hz. Once again, the phase voltages exhibits negligible harmonic content.

Furthermore, Equation 2.16 derived from the theory establishes that the effective values of the respective output line voltages should amount to $306.2\,\mathrm{V_{RMS}}$ for an amplitude modulation index of 1.0, and $153.1\,\mathrm{V_{RMS}}$ for a modulation index of 0.5. This alignment is also evident when examining Figures 8.12d and 8.13d from the laboratory experiments, where the quadratic mean values is tabulated in Table 9.1.



(a) FFT of filtered phase voltages. **(b)** FFT of filtered line voltages.

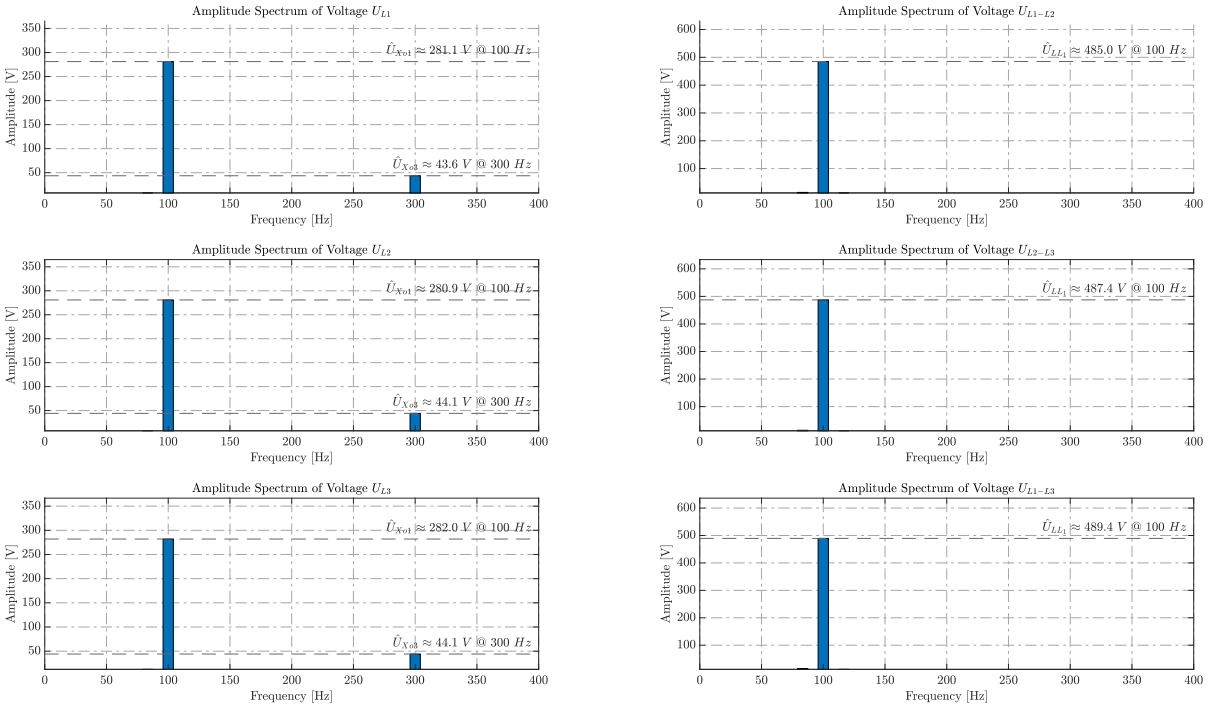
Figure 9.1: Fast Fourier Transform of SPWM generated voltages (data from the experiments conducted in Figure 8.10).
Source: Created using MATLAB (data from oscilloscope).

In the case of SV-PWM, corresponding calculations are carried out based on Equations 2.15 and 2.17. For an amplitude modulation index of 1.0 and an available DC-link voltage of 500 V_{DC}, the theory predicts the fundamental amplitude of the output phase voltages to be 288.7 V. Similarly, for a modulation index of 0.5 , an expected amplitude of 144.3 V is anticipated. These theoretical predictions are validated by Figures 8.12b and 8.13b, which demonstrate measurement results almost consistent with the theoretical expectations. As can be seen, these voltages are higher than the corresponding voltages depicted in Figures 8.10b and 8.11b, generated by the SPWM modulation technique.

Moreover, Figures 8.12b and 8.13b also reveal that the phase voltages contain the same third harmonic frequency component as depicted in Figure 7.3, discussed in Chapter 7.3, which is three times the modulation frequency. For a modulation frequency of 100 Hz, this component is measured at 300 Hz, while for a modulation frequency of 50 Hz, it is measured at 150 Hz. Despite the considerable amplitudes associated with these third harmonic components, which in turn augment the harmonic content present in the phase

voltages, it is this very characteristic that empowers SV-PWM to generate elevated voltages within its linear operating range, in contrast to SPWM.

By comparing Figures 8.12c and 8.13c with Figures 8.12d and 8.13d, it is evident that the third harmonic component is absent in the line voltages, which now consist of three pure sinusoidal waveforms with minimal harmonic content. Furthermore, it can be observed from Table 9.1 that the measured effective values of these voltages is close to the values predicted by Equation 2.17 from the theory. The discrepancies encountered can be attributed to numerous minor harmonic components that are not shown in figures.



(a) FFT of filtered phase voltages. **(b)** FFT of filtered line voltages.

Figure 9.2: Fast Fourier Transform of SV-PWM generated voltages (data from the experiments conducted in Figure 8.12).
Source: Created using MATLAB (data from oscilloscope).

As evident by a comparison of Figures 9.1 and 9.2, SV-PWM outperforms SPWM in terms of generating the highest output voltage. Through the utilization of third harmonic injection, the output line voltages can be approximately 15 % higher without compromising harmonic content. However, it is important to consider that this modulation technique requires additional computational power, and the choice of algorithm should be based on a cost-benefit analysis.

Discussion and Conclusion

This bachelor's thesis presented the development of a three-phase two-level inverter capable of converting direct current (DC) to alternating current (AC) using two different modulation techniques. The report elucidated the fundamental theoretical principles governing the selection of appropriate power electronics, complemented by a series of laboratory experiments that substantiated the theoretical framework while evaluating the inverter's capability in regulating the speed and torque of the induction machine.

The outcomes of this report firmly established that the choice of modulation algorithm significantly influenced the output voltage of the inverter, thereby impacting its overall performance and efficiency. The laboratory experiments confirmed that the Space Vector Pulse Width Modulation (SV-PWM) algorithm utilized the available DC-link voltage more effectively compared to the Sinusoidal Pulse Width Modulation (SPWM) approach, without requiring operation in the overmodulating region.

Furthermore, the measurements also revealed that the selection of different values for the transistors' gate resistors influenced various factors such as power dissipation and switching response. Lower resistor values were found to result in faster switching, which consequently lowered the power losses. However, it was also observed that lower values led to higher peak currents during switching transitions, potentially posing negative implications for the transistors' lifespan.

Although the laboratory testing yielded positive results, demonstrating the overall effectiveness of the design, it is imperative to recognize its limitations and identify opportunities for enhancement. Consequently, a recommended course of action could involve conducting more extensive and rigorous laboratory experiments to comprehensively evaluate the

inverter's performance over extended continuous periods.

In conclusion, this thesis successfully demonstrated the practical application of power electronics in designing a power converter capable of converting DC to AC for controlling the speed and torque of the induction machine. The authors earnestly hope that those who find this report compelling will continue to build upon the resources developed within this project.

Suggestions for Further Work[1]

As a result of time constraints, the inverter designed in the context of this project exhibits areas where further refinements could be made. These suggested enhancements are delineated in the ensuing sections, in addition to recommendations for laboratory experiments that would be relevant to educational objectives.

9.4 Circuit Board Design

As outlined in Appendix B.15, multiple flaws were discovered and identified in the initial version of the circuit board. The deviation log in Appendix B.14 provides details on the faults encountered during testing and a brief description of the actions taken to rectify them. Furthermore, certain components and circuits have not been addressed in a timely manner due to time constraints and their lower priority compared to other more critical tasks.

The brake circuit on the circuit board lacks complete design and simulation concerning hysteresis and the analog comparator, as indicated in Appendix B.8. Some component values remain uncalculated, preventing the testing of the brake circuit within the system. Additionally, the functionality of the brake IGBT's gate driver has not been verified. To ensure the safety of the inverter, it is strongly advised to thoroughly design this subsystem and conduct comprehensive functionality testing, before employing the inverter in a laboratory environment.

[1] The official project files are available for access through the project's GitHub repository

The present configuration of the inverter is designed for current measurements up to $5\,A_{RMS}$, encompassing both the DC-link and the output RMS current. However, this results in suboptimal resolution concerning the microcontroller's analog-to-digital converter due to the choice of components designed for currents up to $50\,A_{RMS}$, which was a requirement specified during the project's initiation[2]. In light of the revised requirement stated in Table 3.1, a potential avenue for enhancement is to replace the current sensors with sensors that possess the appropriate measuring range. This modification would contribute to a higher degree of precision in the readings acquired by the microcontroller. Moreover, the interface between the microcontroller and the current sensors intended to be pinheaders and external wires. A better solution could be ribbon cables and suitable connectors and plugs.

Furthermore, the circuit measuring the DC-link voltage has not been fully tested, due to the lack of an operational amplifier. The isolation amplifier shown in Appendix B.11 has been tested and outputs the correct voltage, but the scaling for ADC in the microcontroller is not tested.

As mentioned in Chapter 9.2, fine tuning the gate resistor value has not been fully concluded, and it is recommended to ensure both optimal operation and efficiency of the inverter.

For the next version, it is also recommended to relocate the HMI components to be recessed within the inverter's enclosure and make the connection between the HMI and microcontroller modular, such as using a flexible ribbon cable and suitable connectors and plugs. On general basis, there are also several measures that can be taken to significantly reduce the size of PCB. The following recommendations are advised to optimize the design while simultaneously shrinking the size of the inverters enclosure.

The circuit board developed as part of this project has been designed to facilitate the dissipation of regenerated power that emerges during motor braking. A significant enlargement of the inverter necessitates the provision of bidirectional power flow support (Active

[2] The requirement was revised downwards from $20\,A_{RMS}$ to $5\,A_{RMS}$, and to accommodate peak values, components supporting $50\,A_{RMS}$ were selected.

Front End), thereby enabling its use in combination with generator operation.

9.5 Simulations

A potential area for improvement is to refine the calculation method for the junction to case thermal resistance, $R_{\theta jc}$, and total power dissipation P_d, presented in Chapter 6. Despite the current methods providing a reasonable estimate, it is not exempt from limitations. Improvement of total power dissipation could be done calculating a more accurate value for each parameter. Enhancing the accuracy of this calculation could increase the precision of the overall heat sink calculation, thereby enhancing the practical application of the results.

Another optimization could employ a simulation in LTspice of SV-PWM with all three phases to increase the validity and generalizability of the system. Incorporating a comprehensive simulation that includes accurate measurements of power dissipation and temperature of transistors would facilitate a more precise analysis of the system's performance. Additionally, including a simulation of the transistors at nominal operating conditions with and without a heat sink would provide a demonstration of the significance of a reliable heat sink. Therefore, conducting such a simulation would be a valuable direction for further analysis.

As a final point, the system could benefit from further investigation with a simulation of the calculated resistors in parallel with the DC-link capacitors. Incorporating a thorough simulation would provide valuable insights into the reliability of the design. A comprehensive simulation would enable the identification and mitigation of potential issues, resulting in an improved and more robust design.

9.6 Software Development

An area that presents potential for improvement within the microcontroller program code is the inclusion of multiple modulation algorithms. This integration would augment

the inverter's versatility in educational laboratory settings, providing an opportunity to compare and contrast different techniques. Moreover, it would be beneficial to establish an algorithmic response for cases in which the amplitude modulation index, m_a, exceeds 1.0 while utilizing both the SPWM and SV-PWM technique.

Another area of potential improvement is the incorporation of motor control functionalities into the program code, such as those discussed in Chapter 1.2. These functionalities would greatly enhance the practicality of the inverter in laboratory settings, allowing adjustments of parameters such as speed and torque.

Likewise, the existing version of the program code lacks the implementation of current and voltage measurements, along with the computation of their average and RMS values. Consequently, the inverter's functionality is currently limited with respect to safety features, as well as general reading of electrical data.

Furthermore, it would be advantageous to establish a more advanced state machine for the human-machine interface than what is currently in place, as this would reduce the inverter's dependence on a computer and streamline its operation. This necessitates interlinkages among the push buttons, the encoder, the display, and the LEDs, enabling adjustments of parameters such as desired voltage, frequency, error message threshold, and other related settings.

In general, enhancing the efficiency of the program code would yield significant benefits in terms of faster processing and reduced resource consumption. Achieving this goal necessitates a deeper understanding of programming in C beyond what has been achieved in this project.

9.7 Laboratory Experiments

Based on the tests conducted in Chapter 8, emphasis has been placed on testing the fundamental functions of the inverter. Placing a greater emphasis on motor operation would allow a more thorough assessment of the inverter's capability to withstand varying loads, regulate speed and torque, and adeptly handle unexpected operational scenarios.

Furthermore, there has been no verification conducted to ascertain the inverter's ability to manage the regenerative power arising from generator operation as discussed in Chapter 1.3. This verification is critical in assessing the functionality of the designed braking circuit.

Moreover, to ensure the proper functionality of the voltage measurement circuit, it is desirable to conduct a test aimed at verifying the DC-link voltage and measuring the amplitude of ripple, with the purpose of corroborating its compliance with the calculated values presented in Chapter 5.3 concerning the dimensions of the DC-link capacitors.

Also, once an algorithmic response of the different modulation techniques has been defined for their overmodulating region, it would be of great interest to conduct a comparative analysis of the harmonic content in relation to the tests conducted in Chapter 8.2 with $m_a \leq 1.0$.

Generally, there are advantages to conducting tests over longer time periods than those covered in this project, as it has the potential to uncover faults or contribute to deviations that are not possible with the tests presented in Chapter 8.

Appendices

Appendix A

Project Management

This appendix outlines the methodology that was employed to effectively manage and execute the various activities of the project.

A.1 Team Coordination

The project, which was conducted between January and May 2023, entailed a series of interrelated activities that spanned the planning, development, and testing phases. Marius Englund[1] was appointed as the project leader and took on the overall responsibility of overseeing the project's progression, and was responsible for both structuring and formulating the report. Nonetheless, the successful completion of the project was a result of the collective efforts of all group members, each of whom was assigned specific tasks and responsibilities.

Eirik Skorve Haugland[2] was accountable for producing technical drawings that conformed to the established specifications, thereby enabling the procurement of the printed circuit boards. This was a critical first step in laying the foundation for the rest of the project. Additionally, he was responsible for developing testing procedures, allowing for verification of the design.

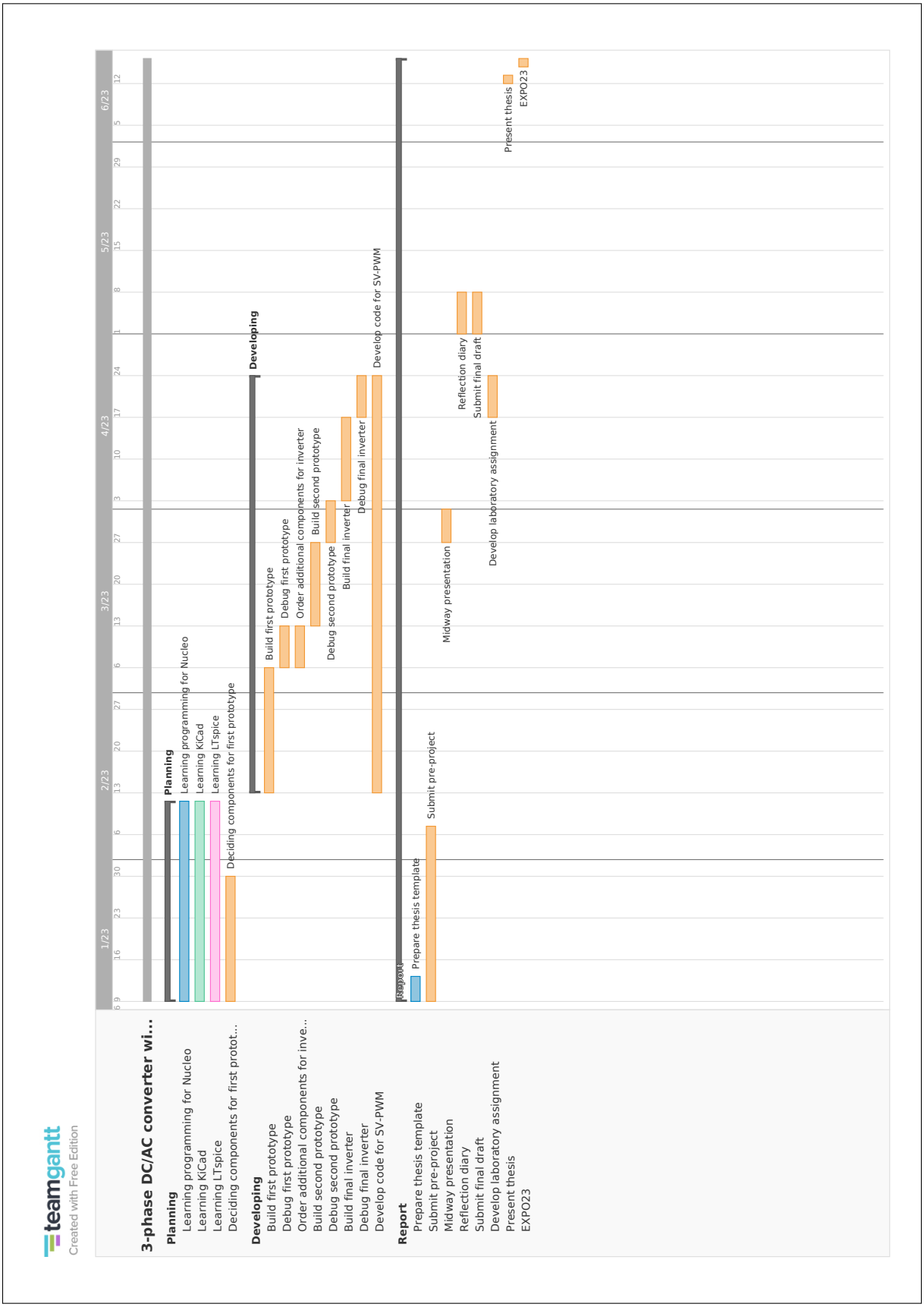
Ingrid Hovland[3] was assigned the task of performing thermal calculations, simulating the design, and overseeing the identification and implementation of necessary modifications prior to ordering. Besides, she was responsible for compiling a record of proceedings from meetings with the supervisor, providing a valuable resource throughout the project.

Marius Englund[1], in addition to his overarching roles, was in charge of implementing the algorithms in the microcontroller, which was a cruical component in meeting the functional requirements of the design. Furthermore, he was responsible for facilitating external access to project materials, simplifying the process of further development.

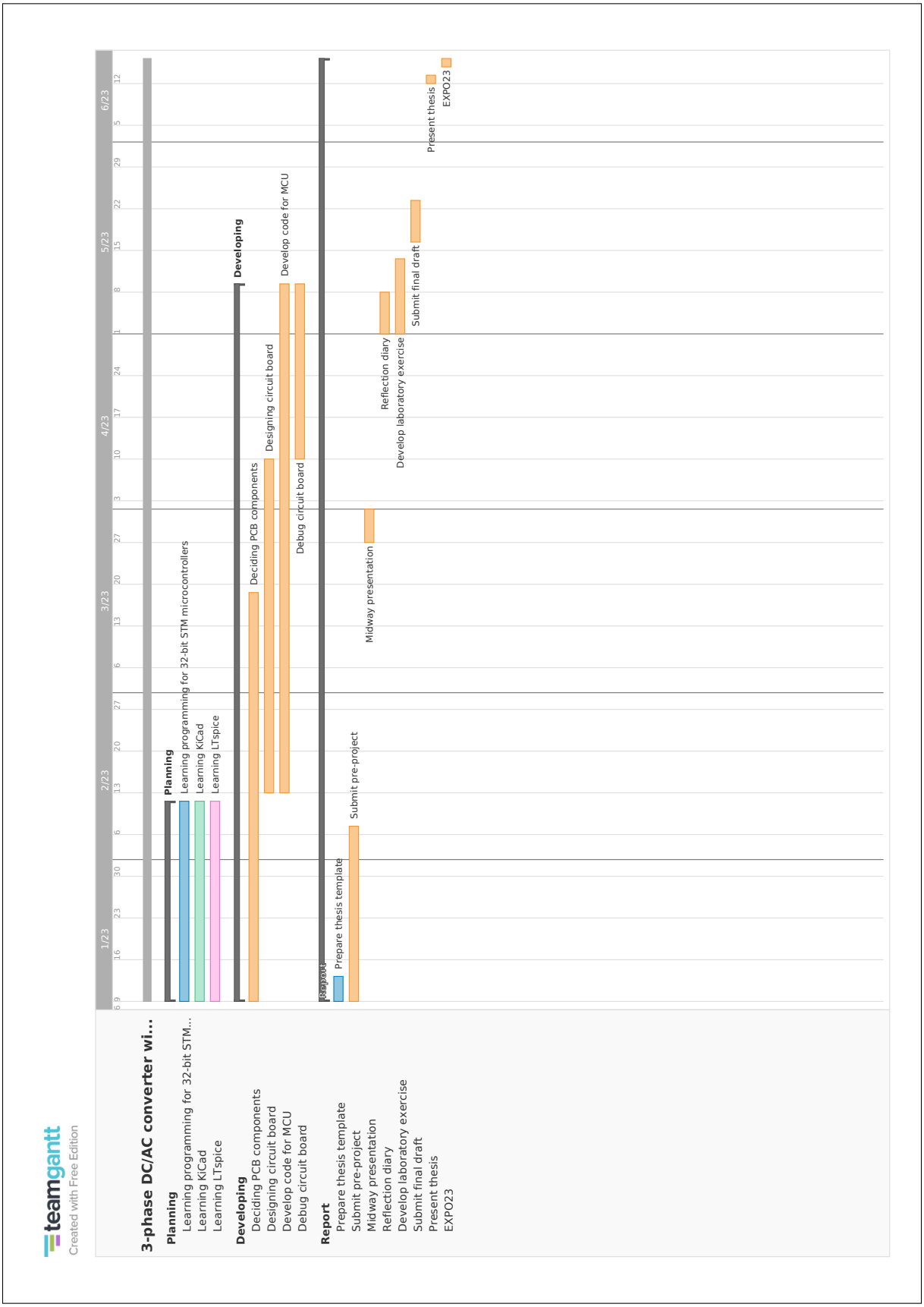
In conclusion, this project serves as a testament to the value of teamwork and collaboration. The combined efforts of all group members were essential in achieving the successful completion of the project.

[1] View Marius's LinkedIn profile here
[2] View Eirik's LinkedIn profile here
[3] View Ingrid's LinkedIn profile here

A.2 Predicted Time Schedule



A.3 Actual Time Schedule



Appendix B

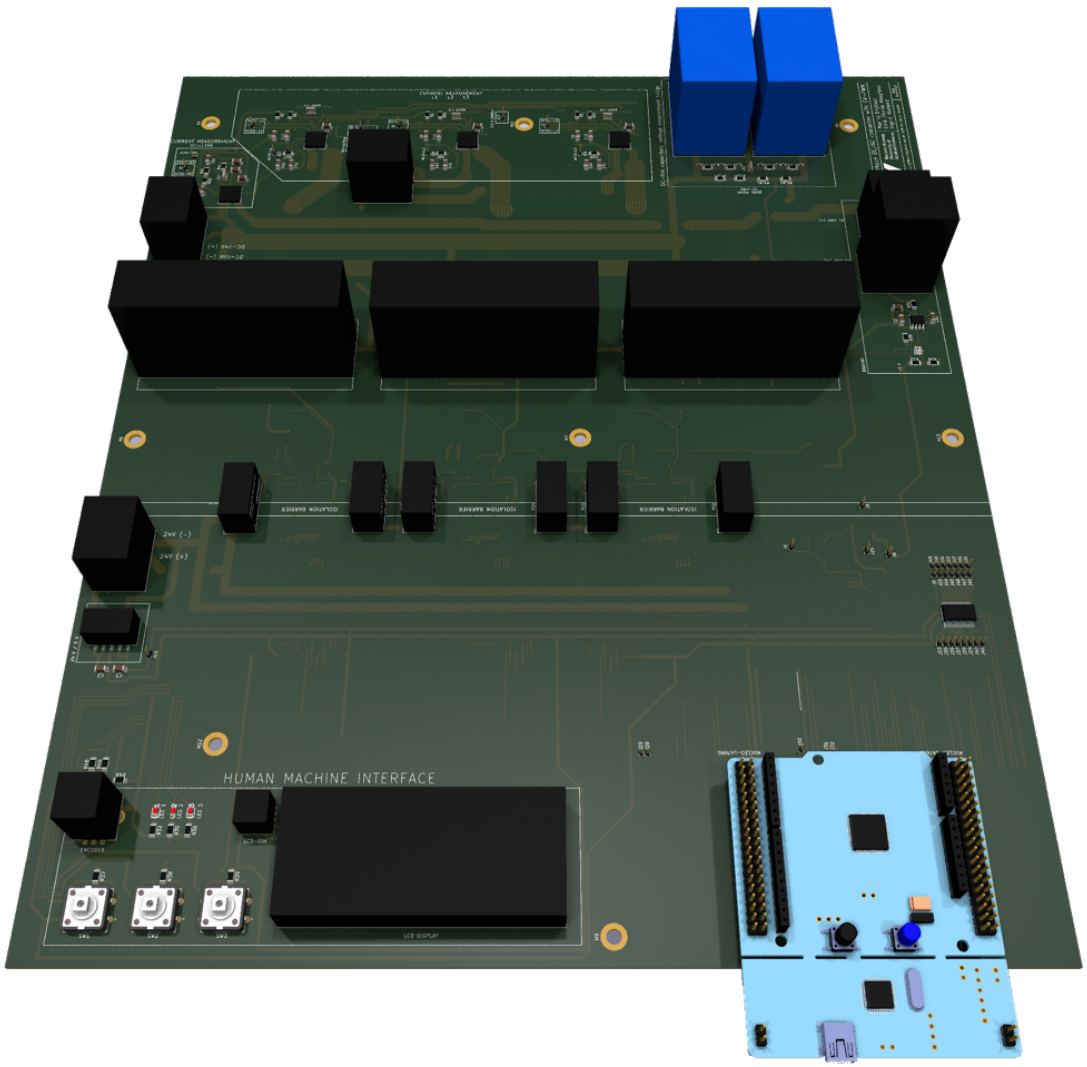
Circuit Board Design

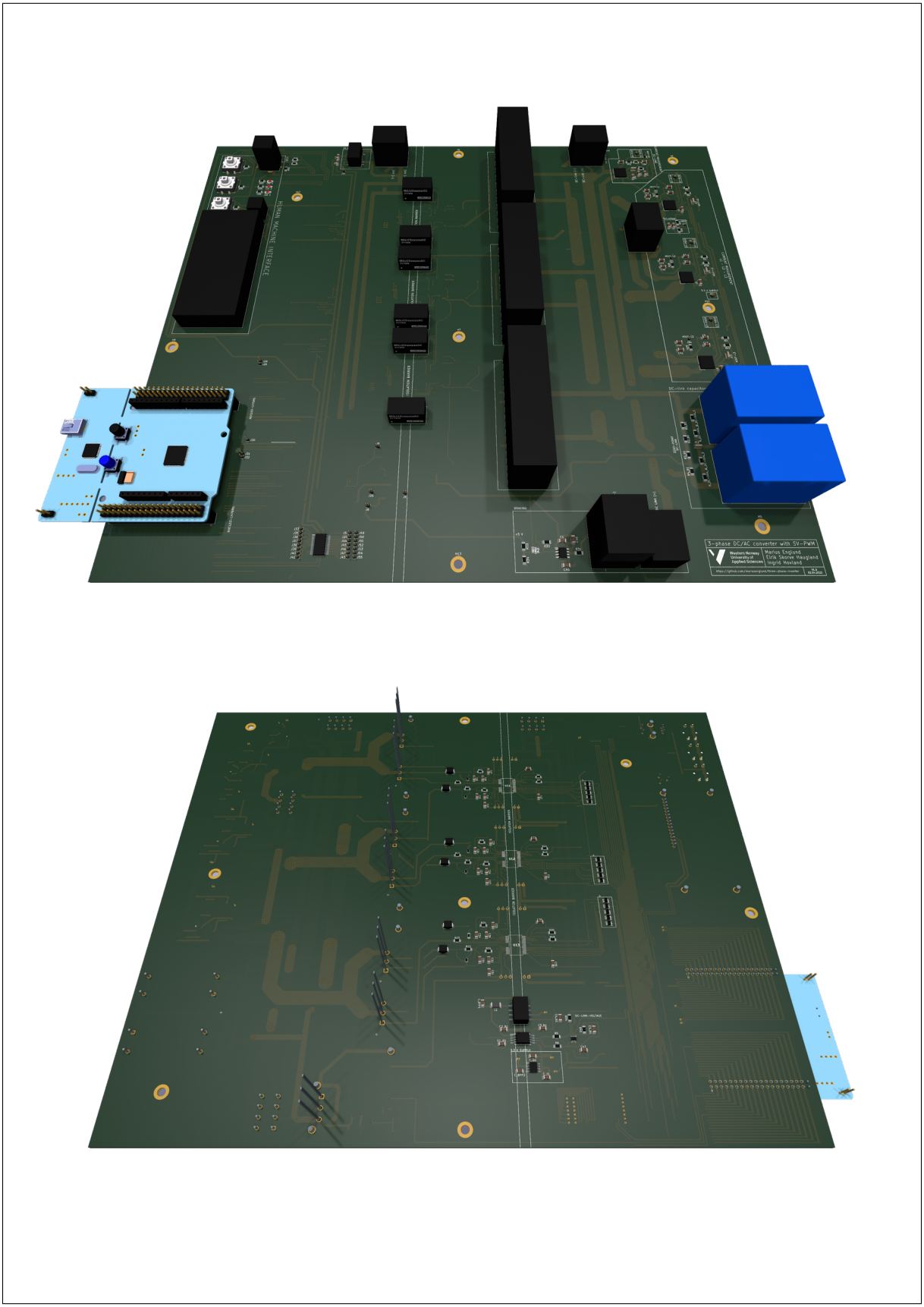
This appendix provides a comprehensive account of the inverter design, encompassing visual documentation of its successful execution, 3D models, PCB layout, circuit diagrams, a detailed component list, a record of resolved deviations, a list of identified design flaws, and a script for calculating DC-link capacitors. The design was developed using KiCad[1].

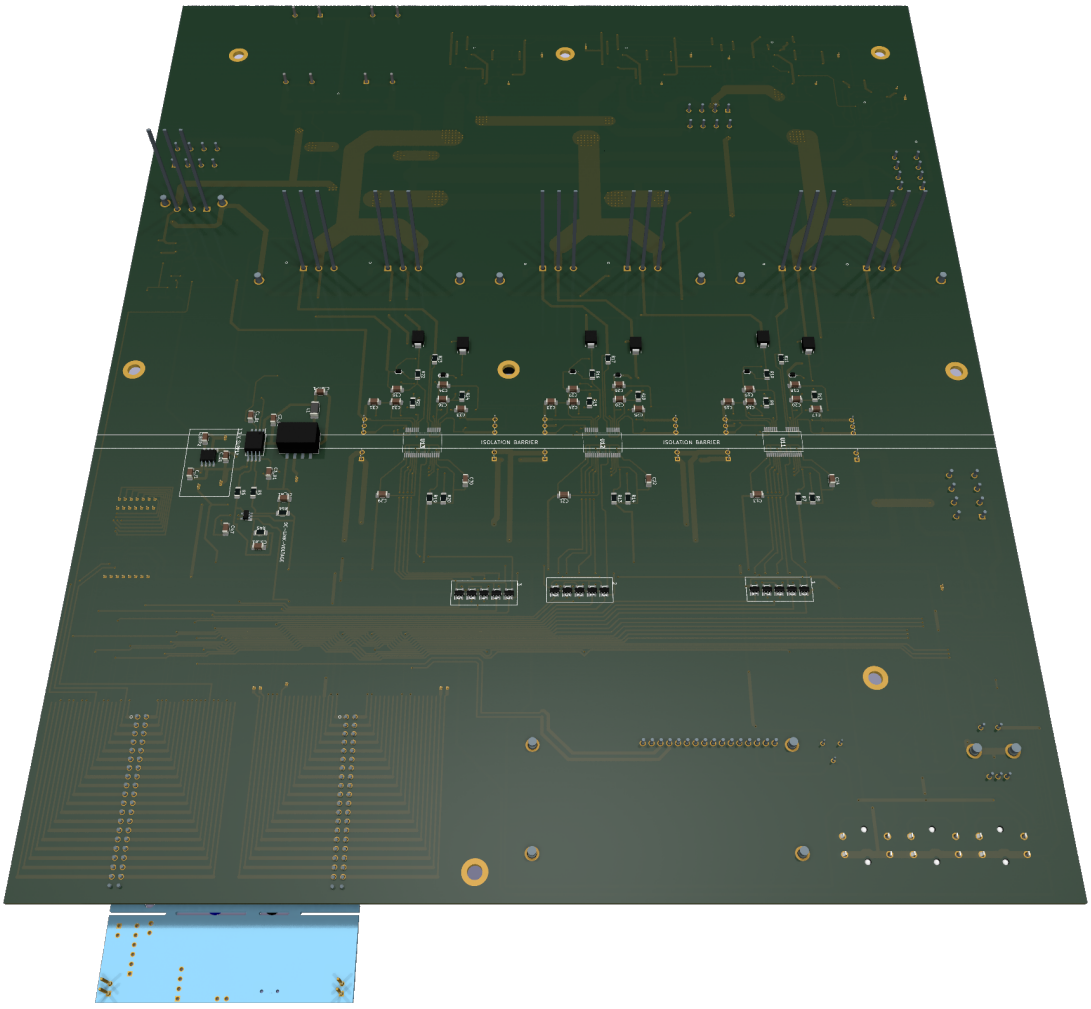
[1] The KiCad project is available on GitHub

B.1 Visual Proof of Execution

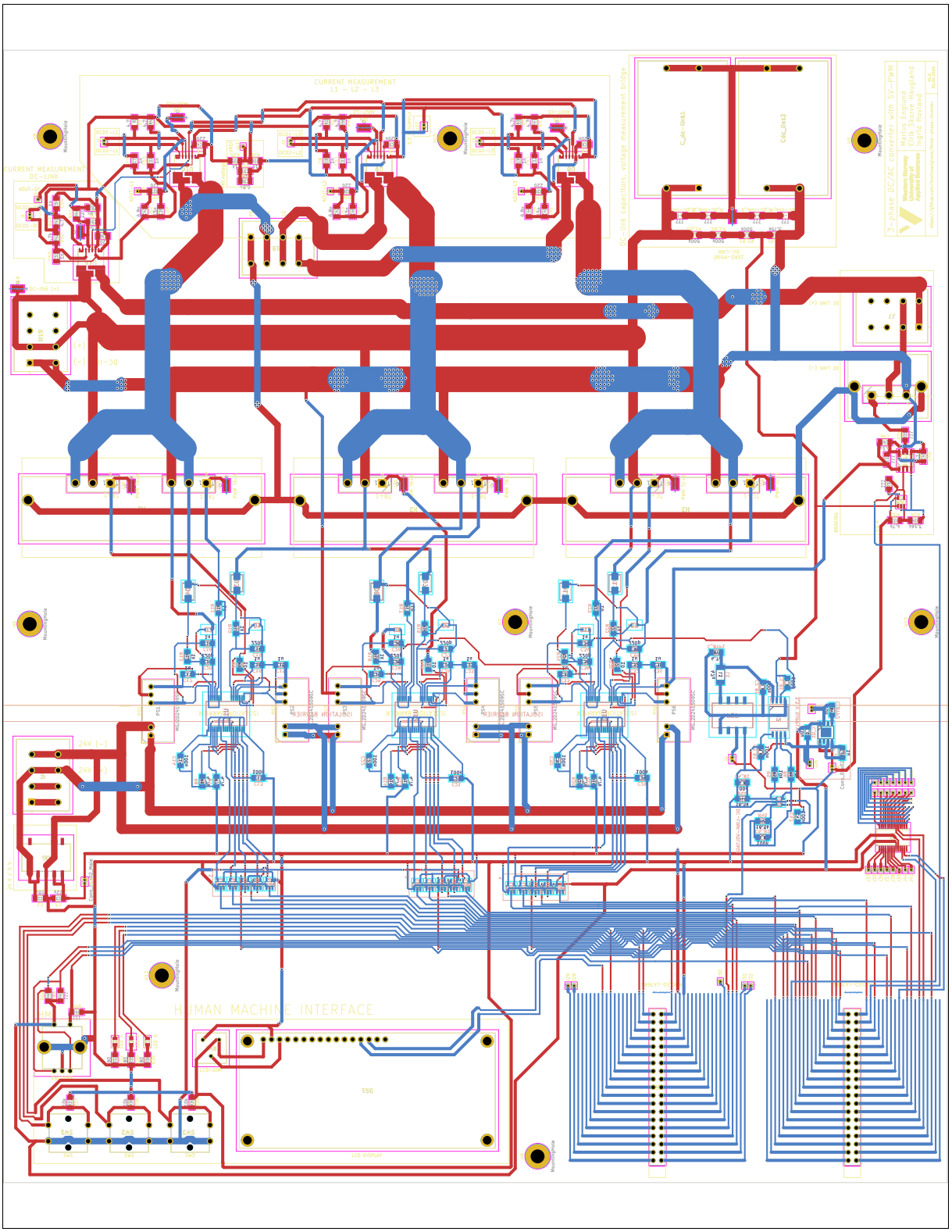
B.2 3D-Models



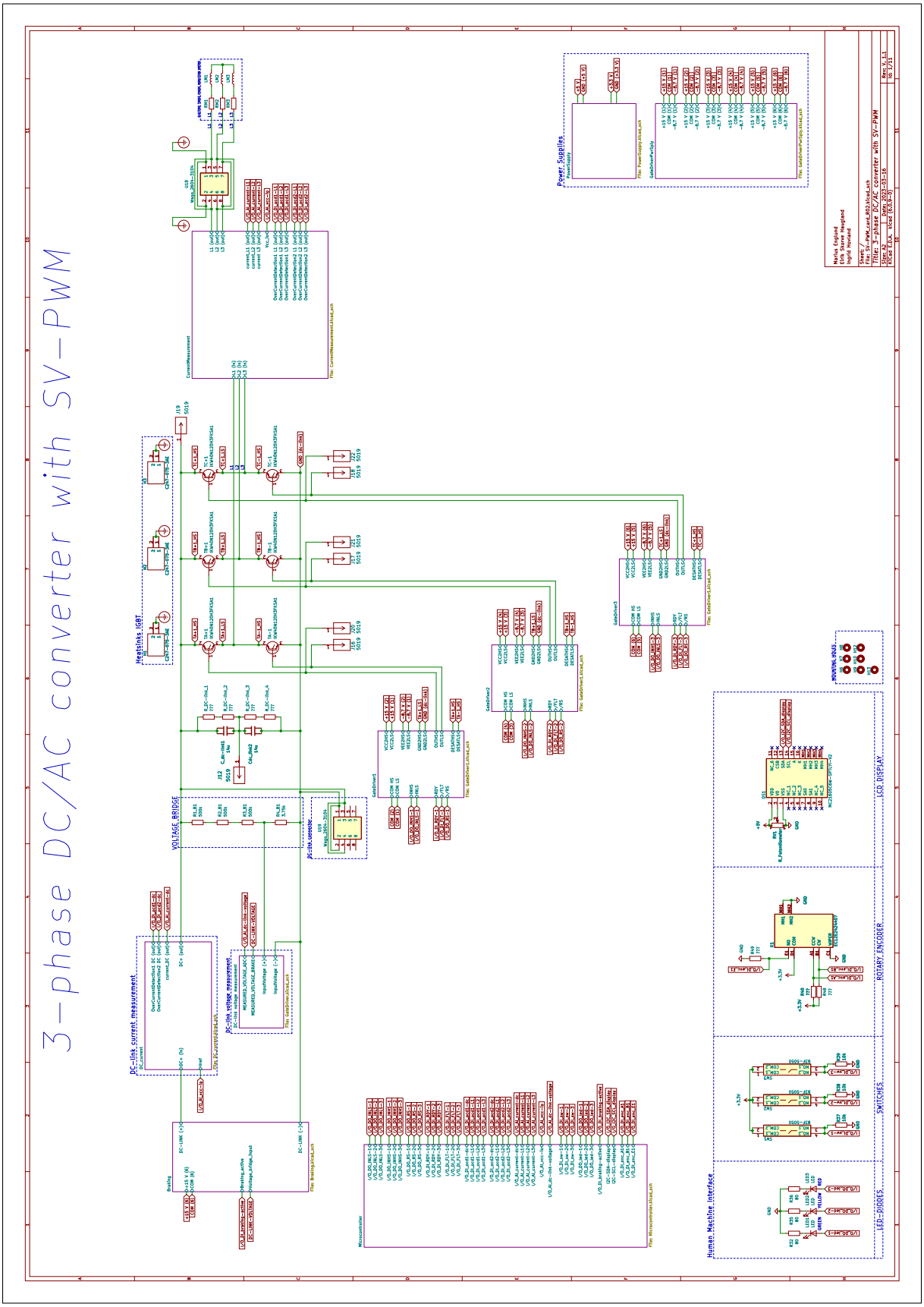

3-phase DC/AC converter with SV-PWM
Western Norway University of Applied Sciences
Marius Englund
Elrik Skorve Haugland
Ingrid Høyland


ISOLATION BARRIER
ISOLATION BARRIER

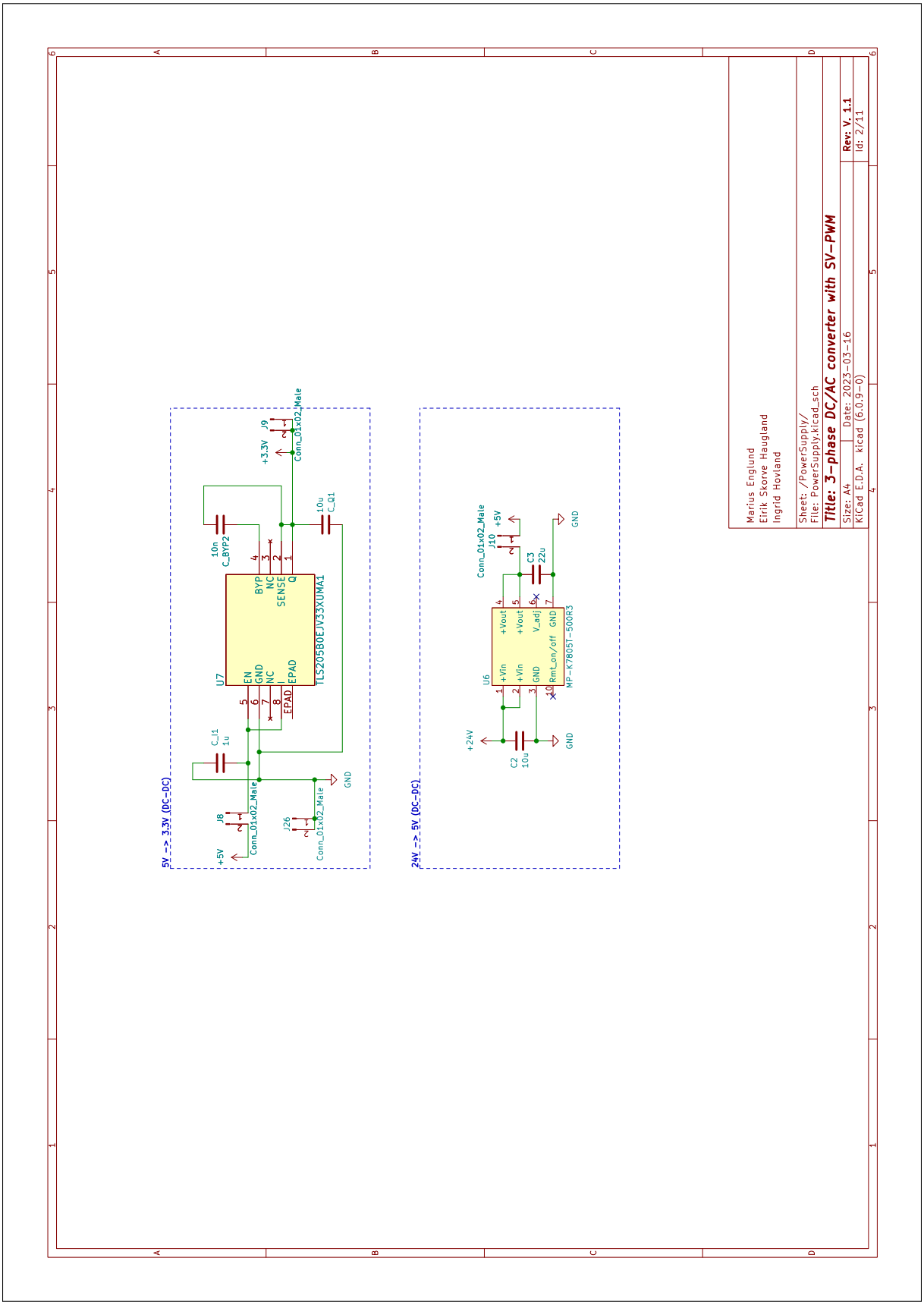
B.3 PCB Layout



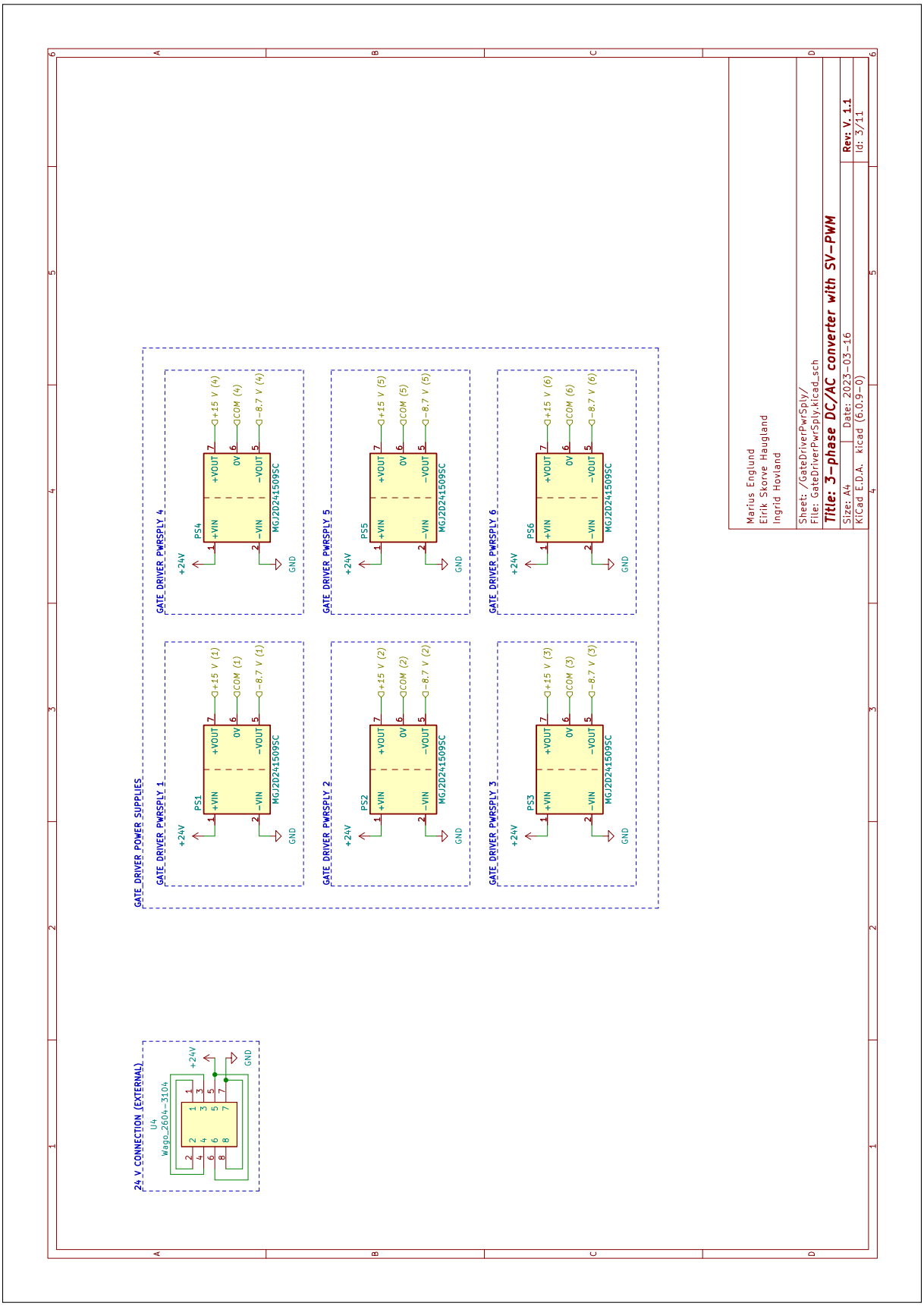
B.4 PCB Topology



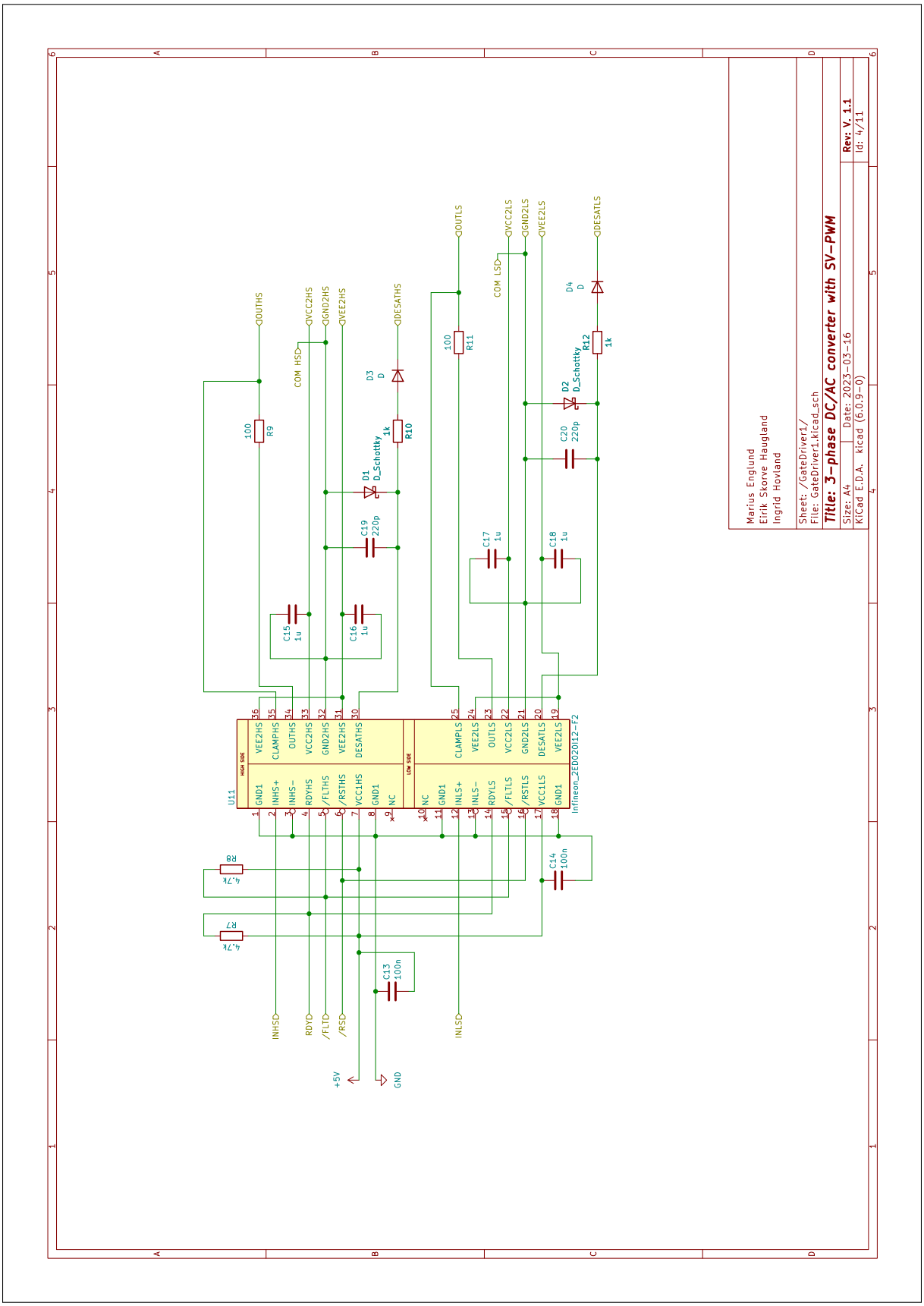
B.5 Power Supply Circuit

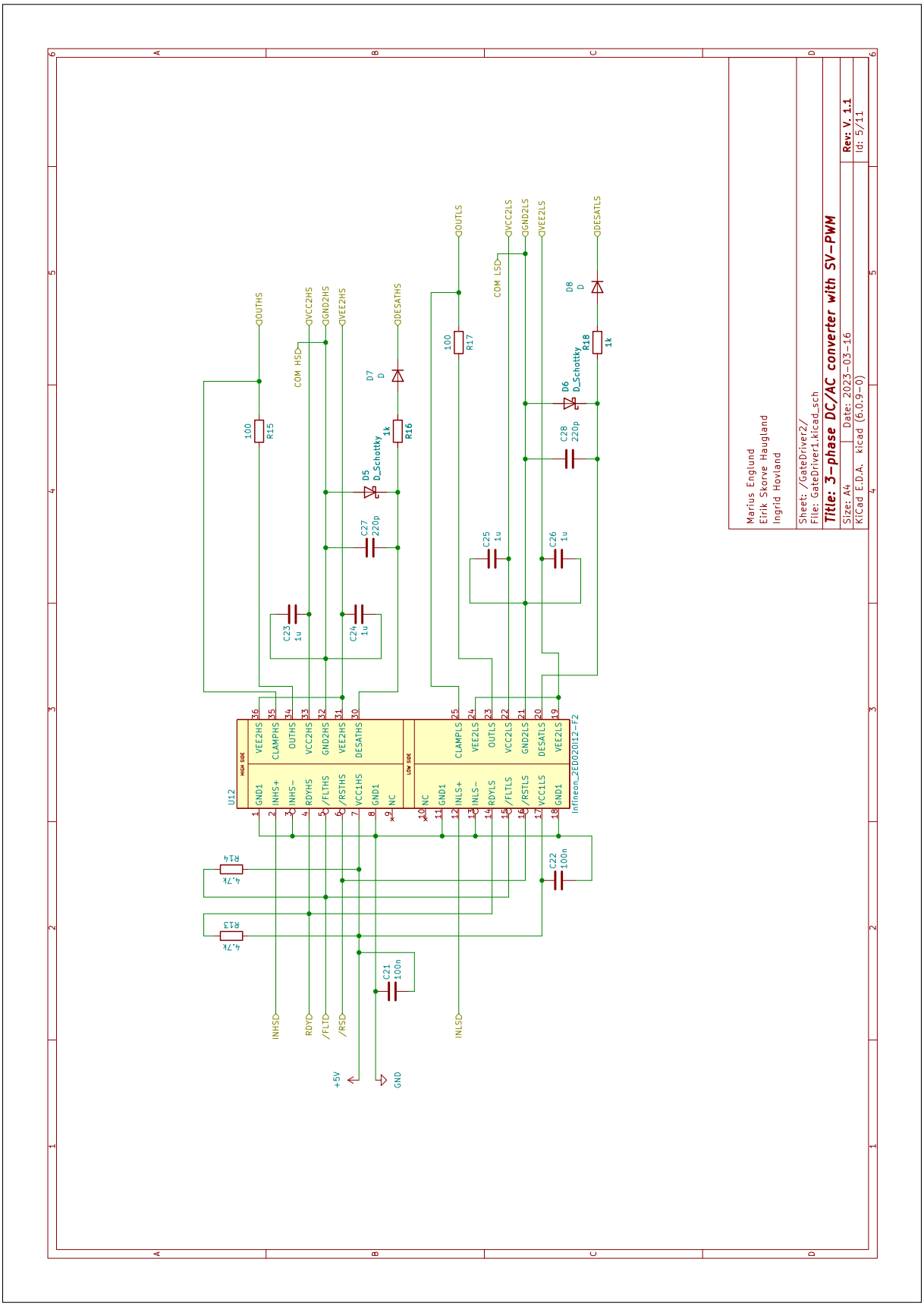


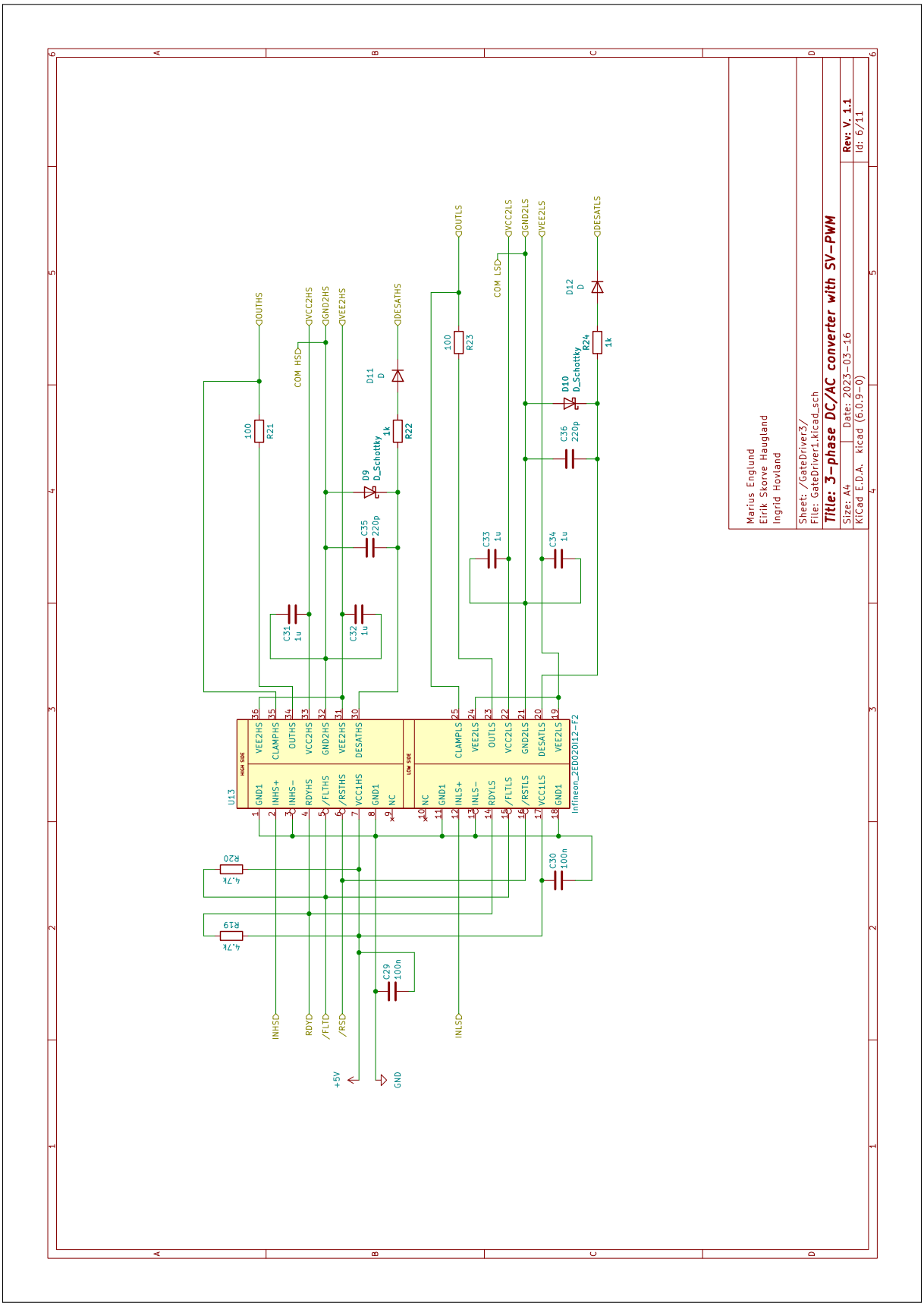
B.6 Gate Driver Power Supplies



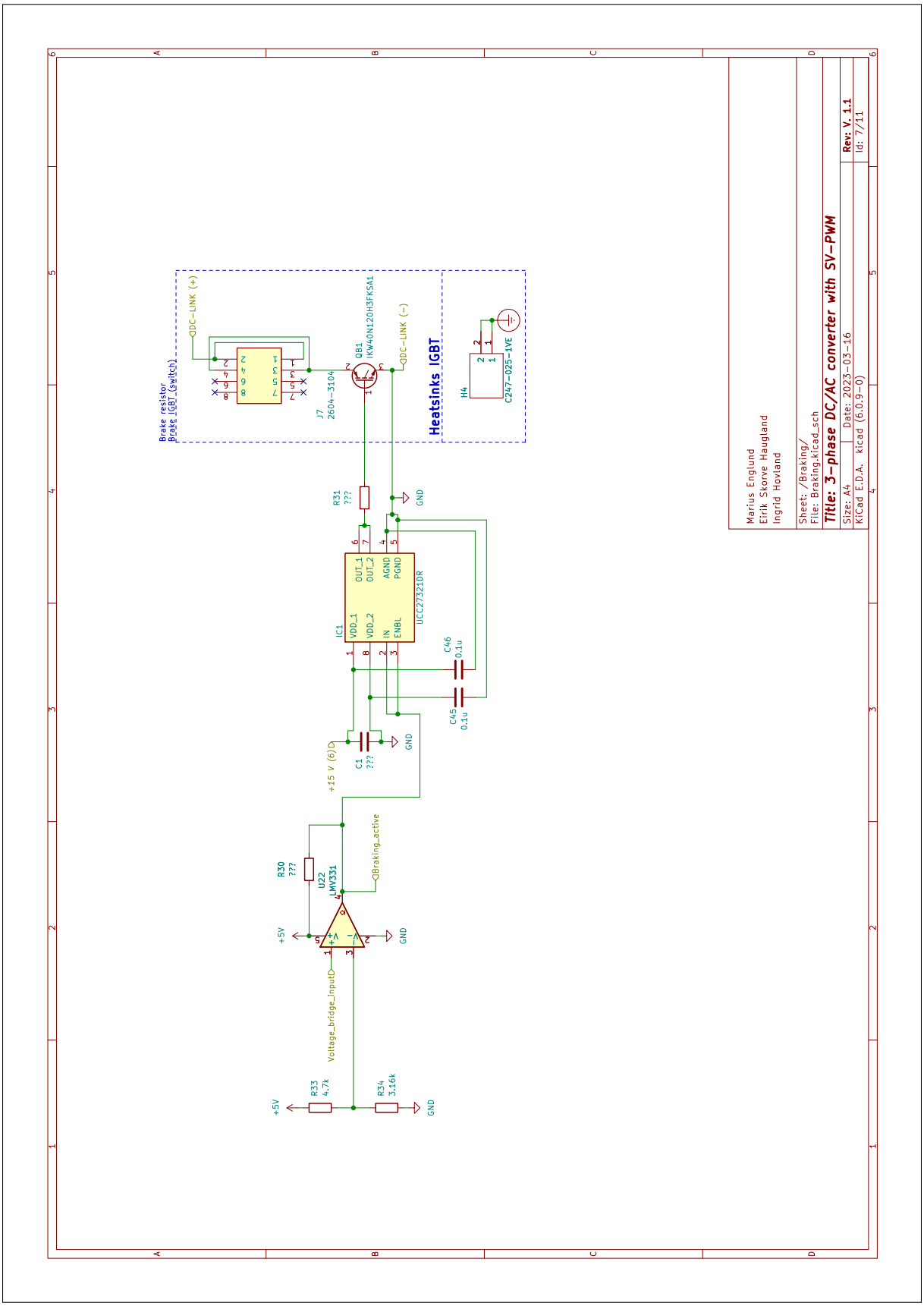
B.7 Gate Driver Circuits



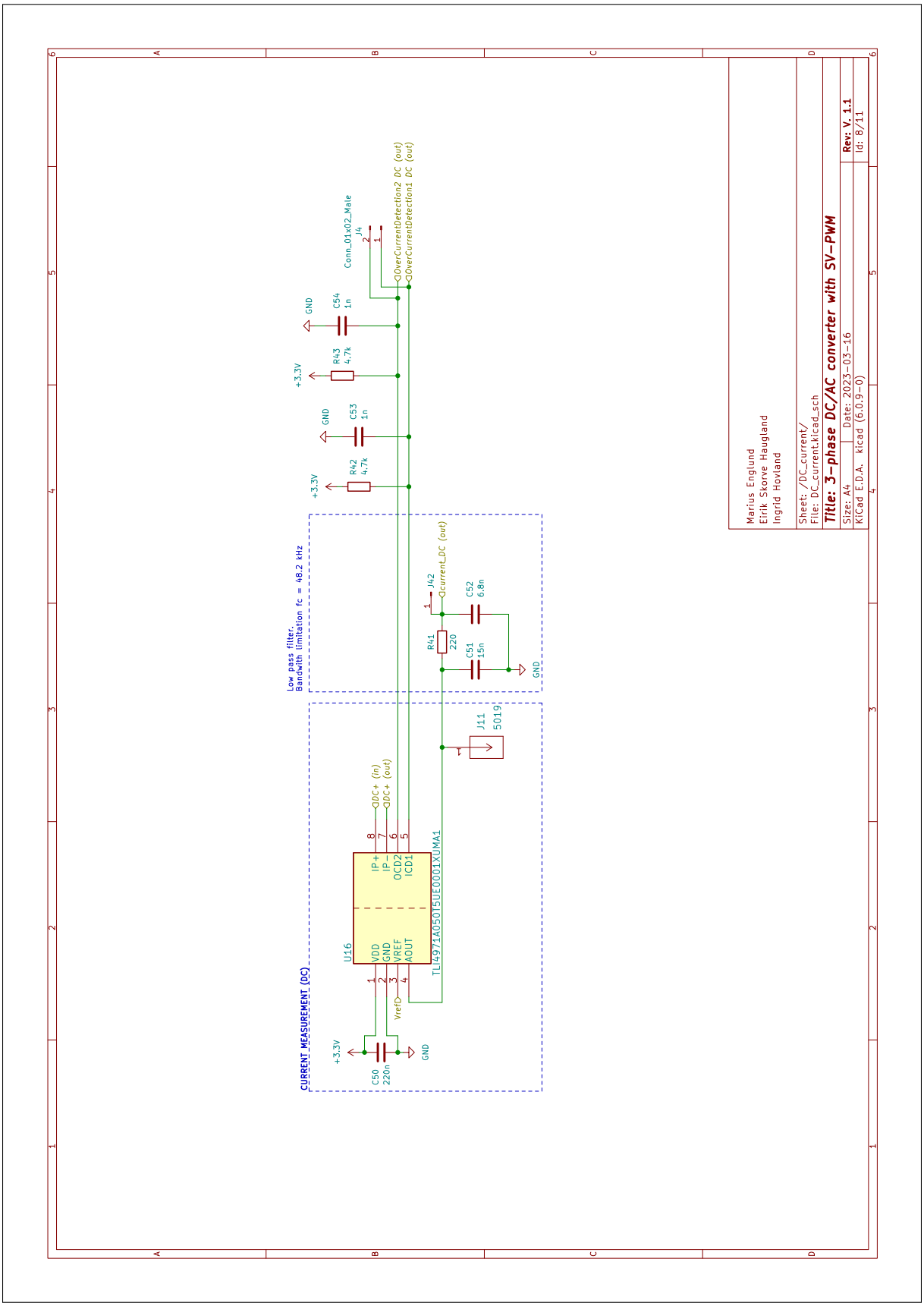

Marius Englund
Eirik Skorve Haugland
Ingrid Hovland
Sheet: /GateDriver2/
File: GateDriver1.kicad_sch
Title: 3-phase DC/AC converter with SV-PWM
Size: A4
Date: 2023-03-16
Rev: V. 1.1
KiCad E.D.A. kicad (6.0.9-0)
Id: 5/11
U12
Infineon_2ED020I12-F2
R15 100
R16 1k
R17 100
R18 1k
R13 4.7k
R14 4.7k
C21 100n
C22 100n
C23 1u
C24 1u
C25 1u
C26 1u
C27 220p
C28 220p
D5 D_Schottky
D6 D_Schottky
D7 D
D8 D
COM HSD
COM LSD
OUTHS
OUTLS
VCC2HS
GND2HS
VEE2HS
DESATHS
VCC2LS
GND2LS
VEE2LS
DESATLS
INHSD
RDYD
/FLTD
/RSD
INLSD
+5V
GND


Marius Englund
Eirik Skorve Haugland
Ingrid Hovland
Sheet: /GateDriver3/
File: GateDriver1.kicad_sch
Title: 3-phase DC/AC converter with SV-PWM
Size: A4
Date: 2023-03-16
Rev: V. 1.1
KiCad E.D.A. kicad (6.0.9-0)
Id: 6/11
U13
Infineon_2ED020I12-F2
C29 100n
C30 100n
C31 1u
C32 1u
C33 1u
C34 1u
C35 220p
C36 220p
R19 4.7k
R20 4.7k
R21 100
R22 1k
R23 100
R24 1k
D9 D_Schottky
D10 D_Schottky
D11 D
D12 D
INHSD
RDYD
/FLTD
/RSD
INLSD
+5V
GND
COM HSD
COM LSD

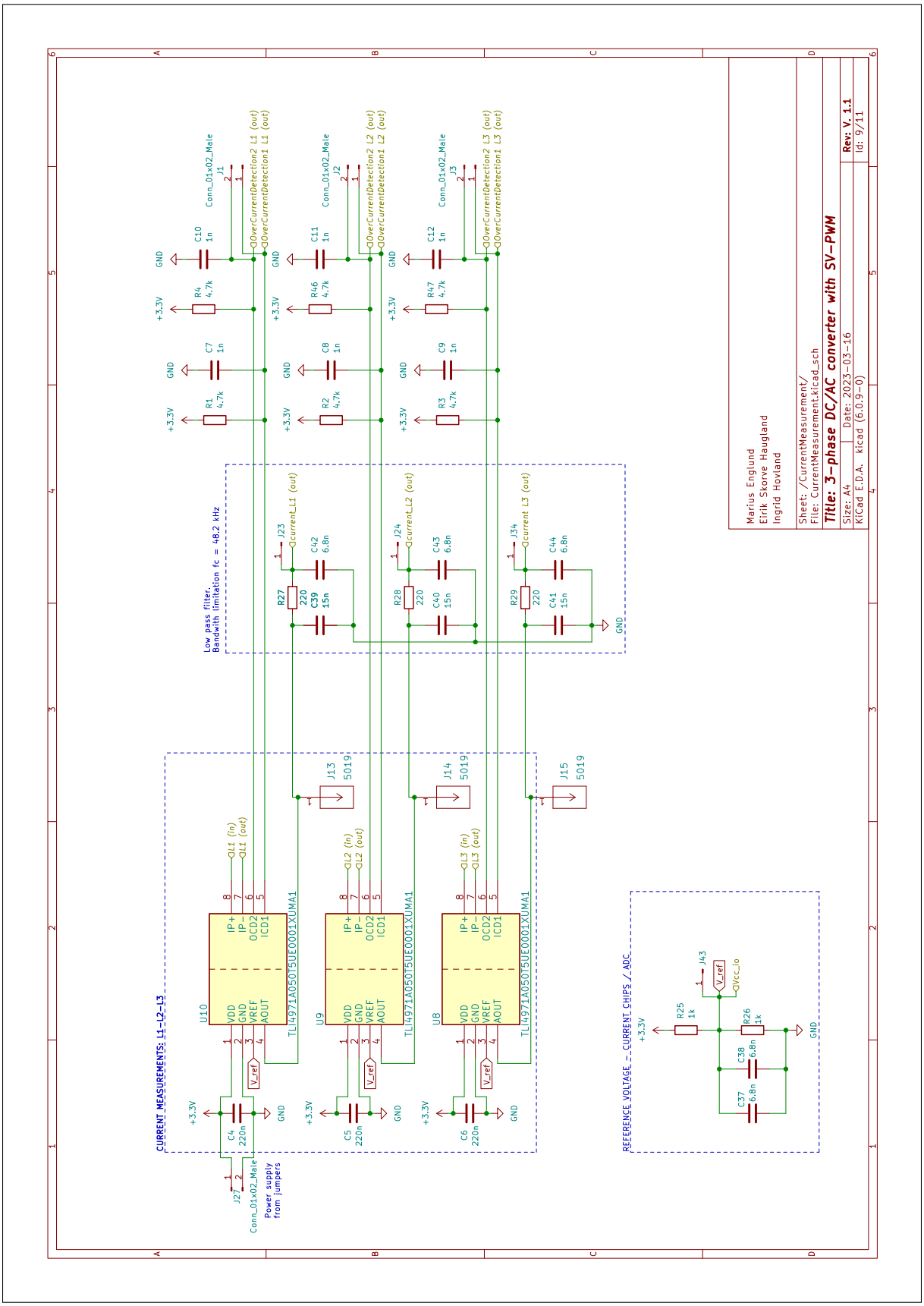
B.8 Braking Circuit



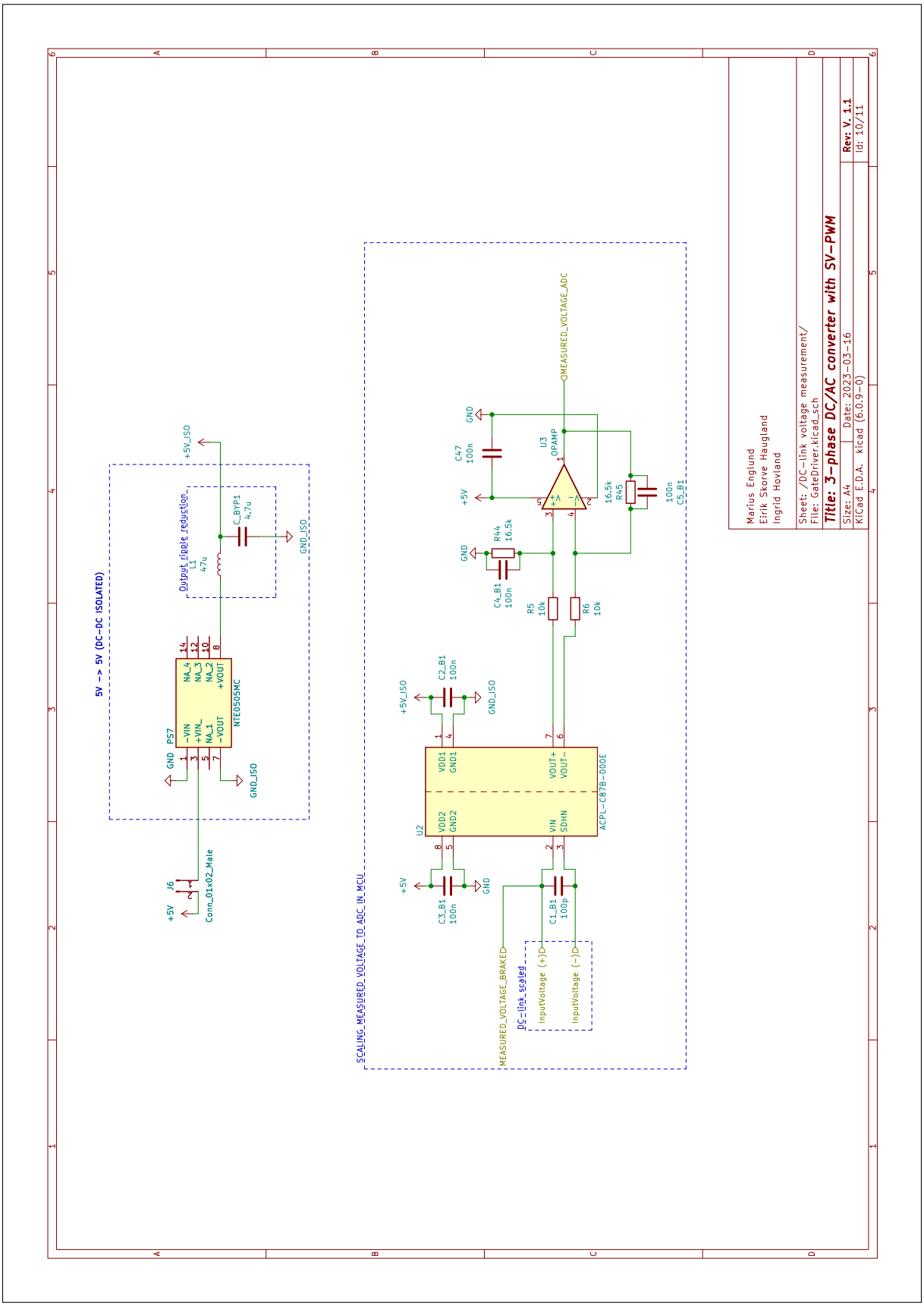
B.9 Current Measurement Circuit (DC)



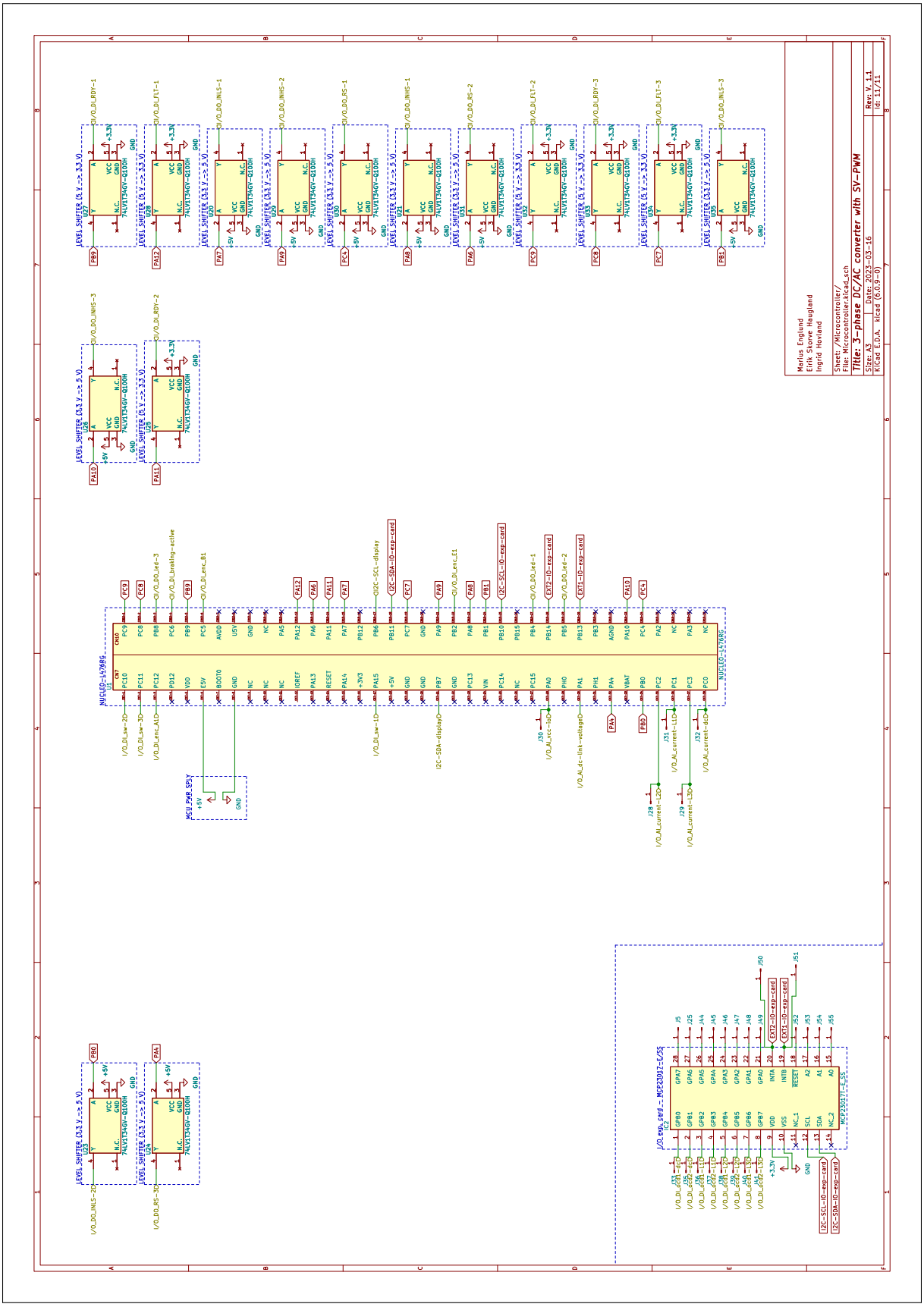
B.10 Current Measurement Circuit (AC)



B.11 Voltage Measurement Circuit



B.12 Microcontroller Circuit



B.13 List of Components

Item	Manufacturer	Model No.	Quantity	Unit Price[1,2,6]
40 x Pin PCB Receptacle	Wurth Elektronik	61304021821	2	NOK 20.66
Analogue Comparator	Texas Instruments	LMV331	1	NOK 11.26
Capacitor 100p	KEMET	C1206X101KGGAC AUTO	1	NOK 10.64[3]
Capacitor 220p	KEMET	C1206C221F5GAC AUTO	6	NOK 8.77[3]
Capacitor 1n	KEMET	C1206S102JDGAC AUTO	8	NOK 12.10[3]
Capacitor 6.8n	KEMET	C1206Y103JDRAC AUTO	6	NOK 13.10[3]
Capacitor 10n	KEMET	C1206Y103JDRAC AUTO	1	NOK 13.10[3]
Capacitor 15n	KEMET	C1206C153F5GEC7 210	4	NOK 23.02[3]
Capacitor 220n	KEMET	C1206X224KARAC AUTO	4	NOK 14.87[3]
Capacitor 0.1u	KEMET	12065C103K4T4A	13	NOK 2.92[3]
Capacitor 1u	KEMET	12061C105K4T2A	13	NOK 4.80[3]
Capacitor 4.7u	KEMET	C1206X475J5RAC AUTO	1	NOK 0.01
Capacitor 14u (DC-link)	EPCOS / TDK	B32776G0146K000	2	NOK 115.55[3]
Capacitor 22u	KEMET	1206YD226MAT2A	1	NOK 5.43[3]
Current Sensor	Infineon Technologies	TLI4971A050T5UE 0001XUMA1	4	NOK 77.68

Item	Manufacturer	Model No.	Quantity	Unit Price[1,2,6]
DC-DC Converter 24V/5V	MULTICOMP PRO	MP-K7805T-500R3	1	NOK 34.03
DC-DC Isolated Converter (5V-5V)	Murata Power Solutions	NTE0505MC	1	NOK 82.19
Development Board	STMicroelectronics	NUCLEO-L476RG	1	NOK 150.50
Diode	STMicroelectronics	STTH112U	6	NOK 7.07
Encoder	ALPS ALPINE	EC12E2420803	1	NOK 9.20
Gate Driver	Infineon Technologies	2ED020I12-F2	3	NOK 78.47
Gate Driver Braking Circuit	Texas Instruments	UCC27321DR	1	NOK 15.98[3]
Heat Sink	Ohmite	C247-075-3VE	3	NOK 78.52
Heat Sink Braking Circuit	Ohmite	C247-025-1VE	1	NOK 45.29[3]
IO Expansion Card	Microchip	MCP23017-E/SS	1	NOK 18.09
LCD Module	MIDAS	MC21605C6W-SPTLYI-V2	1	NOK 137.83
LED Green	LUMEX	SML-LX0805SUGC-TR	1	NOK 4.11
LED Red	LUMEX	SML-LX0805SIC-TR	1	NOK 5.42
LED Yellow	LUMEX	SML-LX0805SYC-TR	1	NOK 5.38
Level Shifter	Nexperia	74LV1T34GV-Q100H	15	NOK 5.00

Item	Manufacturer	Model No.	Quantity	Unit Price[1,2,6]
Fixed LDO Voltage Regulator	Infineon Technologies	TLS205B0EJV33	1	NOK 19.11
Operational Amplifier	Texas Instruments	OPA237N/3K	1	NOK 18.95
PCB Standoff M4	Wurth Elektronik	971100471	8	NOK 3.96
PCB Standoff Nut M4	Wurth Elektronik	R40-1000802	8	NOK 4.34
PCB Test Point	Keystone Electronics	5019	12	NOK 3.44[3]
Potensiometer LCD Light	Bourns	3386F-1-203TLF	1	NOK 22.84
Printed Circuit Board	JLCPCB	V1.0	1	∼NOK 1000.00[4]
Push Buttons	Omron	B3F-5050	3	NOK 6.72
PWR Gate Driver	Murata Power Solutions	MGJ2D241509 SC	6	NOK 87.46
Resistor 80	MULTICOMP PRO	MCMR06X1000 FTL	3	NOK 0.01
Resistor 100 (gate)	MULTICOMP PRO	MCMR06X1000 FTL	6	NOK 0.01
Resistor 220	MULTICOMP PRO	MCSR08X2203 FTL	4	NOK 0.04
Resistor 1k	MULTICOMP PRO	MCMR04X1001 FTL	8	NOK 0.04
Resistor 3.16k	MULTICOMP PRO	MCMR04X3161 FTL	1	NOK 0.01
Resistor 3.75k	MULTICOMP PRO	MCWR06X3741 FTL	1	NOK 0.01

Item	Manufacturer	Model No.	Quantity	Unit Price[1,2,6]
Resistor 4.7k	MULTICOMP PRO	MCMR06X4701 FTL	15	NOK 0.05
Resistor 10k	MULTICOMP PRO	MCMR04X103 JTL	5	NOK 0.01
Resistor 16.5k	MULTICOMP PRO	MCWR06X1652 FTL	2	NOK 0.01
Resistor 430k (DC-link)	MULTICOMP PRO	MCWR06X4303 FTL	4	NOK 0.02
Resistor 500k	MULTICOMP PRO	MCWR06X4993 FTL	3	NOK 0.02
Schottky Diode	Nexperia	BAT165AX	6	NOK 4.22
Transistor	Infineon Technologies	IKW40N120H3 FKSA1	7	NOK 94.75
Voltage Sensor	Broadcom	ACPL-C87B-000E	1	NOK 132.52
Wire-To-Board Terminal Block	WAGO	2604-3104	4	NOK 55.40
TOTAL				NOK 4957.67[5]

Table B.1: List of components employed in a single inverter.

[1] The prices listed correspond to the second quarter (Q2) of the year 2023.
[2] Farnell serves as the pricing reference for all components listed, unless otherwise specified.
[3] Cost from Mouser.
[4] Cost from JLCPCB.
[5] The overall cost of the inverter, comprising all components.
[6] The price is subject to variation based on the quantity ordered and associated shipping expenses.

B.14 Deviation Log PCB

Dev. No.	Date	Deviation	Solution
1	17 Apr 2023	After testing card 1 with DC-link up to 30 V and a current draw less than 4 A, the switching suddenly stopped working. Various troubleshooting has been performed, and it has been determined that there is a fault with the IGBT due to excessive current on gate of the IGBT.	After a discussion with the supervisor, the gate resistor in the circuit has been corrected from 10 Ω to 100 Ω.
2	19 Apr 2023	New testing has been conducted with a new gate resistor. PWM is generated from the microcontroller and applied to the gate of the IGBT (confirmed with oscilloscope). The power supply voltage suddenly dropped from 24 V during testing. The isolated DC-DC converter used to power supply gate driver “power side” became warm. However, the current draw at 24 V power supply is normal when the isolated DC-DC converters are disconnected.	Soldering new isolated DC-DC converters to the PCB.
3	19 Apr 2023	New testing has been conducted with new DC-DC converters. But the output voltage of them is not correct. There is suspicion that there might be fault with the gate driver or IGBT.	Project leader is consulting with the supervisor about which components should be replaced to fix the problems and prepare for new testing.
4	19 Apr 2023	Replaced IGBTs, replaced gate driver, and replaced DC-DC converters.	A new test has been conducted and it seems to be working properly. The supervisor needs to approve whether the results are satisfactory before the remaining components of the board gets soldered.
5	21 Apr 2023	It has been tested with a higher DC-link voltage and verified that the IGBT HS and LS are switching with too little delay, resulting in ringing. It has been attempted to make changes to microcontroller’s timer delay, but it had little impact.	Measure INHS+ and INLS+ on the gate driver and OUTHS and OULS to understand how the gate driver is behaving, and what time delay it is.
6	23 Apr 2023	Tested and measured that the outputs of the gate drover are functioning properly. The delay parameter in the timer is used to delay the switching between the upper and lower transistors.	The supervisor needs to verify that the component is functioning properly before giving green light for testing a new complete board.
7	26 Apr 2023	Cut copper traces with the DC-link current sensor. Design flaw, resulting in wrongly routed copper traces. Had to be done to ensure that all main current goes through the current sensor.	Seems successful. Measured output signal of the current sensor that changes with changing current.

Dev. No.	Date	Deviation	Solution
8	27 Apr 2023	Soldered resistors to the voltage divider of the DC-link (voltage measurement). Used 5 V iso power and ACPL galvanically isolated chip. Did not get the expected voltage output of the ACPL chip.	Checked in KiCad and the component's datasheet. Turns out a connection between pin 3 and 4 was forgotten. Soldered it on the chips legs, and it is now 0-1 V out of the chip with the DC-link varying between 0-500 V.
9	03 May 2023	Finished soldering chips and components to all three legs on board number 2. Measured PWM from the microcontroller and on the gate of all the six IGBTs with differential probes. Rgate = 75 Ω. Did not get square pulses on TC- as all the other IGBTs. Troubleshoot to determine the cause of issue.	Two resistors turned out to be swapped causing the gate resistor to be 1 kΩ and desat resistor to be 75 Ω. Swapped the resistors with correct values, and the PWM on gate of TC- looks correct now.
10	08 May 2023	Tested second card with S-PWM and three-phase resistive load. Seems to work fine, but some level shifters got very hot. Seems to be the one translating \FLT signal from driver to microcontroller.	Tried to resolder the components legs. No change.
11	09 May 2023	Soldered new level shifters to the second PCB. Swapped out all level shifters with 3.3 V power supply.	Retested. Seems to work fine. No hot chips.

B.15 Design Flaws PCB

No.	Description
1	Galvanic isolation is broken, 5 V supply to brake circuit. Cut copper trace, and redesign in v2.
2	The pin headers have wrong footprint. They are 1 mm, but should be 2.54 mm. Redesign in v2.
3	3.3 V power supply is not working as it should. Suggestion to change to Multicomp Pro chip (same as 24 V to 5 V) but 3.3 V version. Implement in version 2.
4	Microcontroller is rotated 180° incorrectly compared to what was intended. Signals are correctly routed. Consider redesign in v2.
5	Apply pinout label for microcontroller pins on silk layer.
6	Issue with the DC-link current measurement. Current sensor only measures the braking current. Redesign in v2.
7	Implement wider copper traces on the gate signal (driver to IGBT) to v2.
8	Consider implementing “buffers” to the isolated DC-DC converters supplying the gate drivers (tips from Vegard Steinsland).
9	Low current carrying capability on main trace DC-link to brake circuit. Only one via point. Fix in v2.
10	Isolation amplifier (ACPL) missing connection between leg 3 and 4. See datasheet. Fix in v2.
11	5 V iso supply should be rotated 90° to have galvanic isolation in the galvanic isolation “split” of the card (marked in silkscreen). See KiCad. Fix in v2.
12	Current sensors have a lot of noise on their Aout pin. Find out why and take the results in considerations when designing v2.

B.16 DC-Link Capacitor Calculations

Code B.1: Script for calculation of DC-link capacitors (MATLAB).

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
%   @brief          : Code for calculating size / dimensions of DC-link capacitors
%   @author         : Marius Englund, Eirik Skorve Haugland, Ingrid Hovland
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


clc; clear; close all;

Ud            = 565;    % voltage over one capacitor
fs            = 5000;   % switching frequency

%% calculating motor equivalent impedance
cosfi = 0.7;   % cos fi for typical induction motor
fi = acos(cosfi);
Ic = 5; % current through motor
Ic_fi = Ic*exp(j*fi);
Z = Ud/Ic_fi;
XL = abs(imag(Z)/(2*pi*fs));
R = real(Z);
L = XL/(2*pi*fs);
fprintf("Impedance of motor equivalent = %.2f + %.4fj %c\n",R,XL,char(937))
fprintf("Inductance of motor equivalent = %.2f nH\n",L*(1e9))

%% calculating size of capacitors
ripple = 1;   % allowed ripple in voltage in percent
deltaUd = Ud*(ripple/100);   % voltage ripple peak-peak
L_calc = 5e-3;   % value of LC filter on output
C_tot = Ud/(32*L_calc*deltaUd*fs^2);   % total capacitance
C1 = C_tot/2;   % capacitance for one of the two capacitors
fprintf("Total capacitance = %.2f uF\n",C_tot*(1e6))

%% Calculating I ripple for the capacitor,
I_ripple_pkpk = (0.25*Ud)/(fs*L_calc);   % peak-peak current ripple
I_ripple_RMS  = I_ripple_pkpk/(sqrt(2))/2;   % RMS current ripple
fprintf("Ripple in current (pk-pk) = %.2f A\n",I_ripple_RMS)

%% calculating size of resistors and power developed
C = 14e-6;   % size of chosen capacitor
t = 60;   % discharging time [s]
R = t/(5*C);   % tau = R*C;
R1 = R/2;
fprintf("Resistance for one capacitor = %.2f k%c\n",R/(1e3),char(937))

%% calculating power developed in one resistor
P = (Ud/4)^2 / R1;
fprintf("Power developed in one resistor = %.2f mW\n",P*1e3)
```

Appendix C

Source Code

This appendix presents segments of the program code implemented for the microcontroller used in the inverter, alongside a record of deviations that were identified and solved throughout the testing phase. The code was developed using PlatformIO[1], which was configured to use the STM32Cube framework.

[1] The PlatformIO project is available on GitHub

C.1 Sinusoidal PWM Algorithm

```c
/**
  ********************************************************************************
  * @brief          : Sinusoidal Pulse Width Modulation Algorithm
  * @author         : Marius Englund, Eirik Skorve Haugland, Ingrid Hovland
  ********************************************************************************
  *
  * The all-encompassing code for the inverter is available at:
  * https://github.com/mariusenglund/three-phase-inverter/tree/main/source-code
  *
  ********************************************************************************
  */


/* Calculate Timer Compare SPWM ------------------------------------------------*/
// Returns timer compare values using the Sinusoidal PWM algorithm.
compare_t calculate_timer_compare_spwm(float ma, uint32_t k_reload, uint32_t i1,
                                       uint32_t i2, uint32_t i3) {

  compare_t compare;
  float bias = k_reload;

  if (ma <= 1.0) { // Linear modulation
      compare.L1 = (uint32_t)((ma*k_reload*sine_table[i1]+bias)/2.0);
      compare.L2 = (uint32_t)((ma*k_reload*sine_table[i2]+bias)/2.0);
      compare.L3 = (uint32_t)((ma*k_reload*sine_table[i3]+bias)/2.0);
  }

  return compare;
}
```

Code C.1: Microcontroller code for the Sinusoidal PWM algorithm (C).

C.2 Space Vector PWM Algorithm

```c
/**
  ******************************************************************************
  * @brief          : Space Vector Pulse Width Modulation Algorithm
  * @author         : Marius Englund, Eirik Skorve Haugland, Ingrid Hovland
  ******************************************************************************
  *
  * The all-encompassing code for the inverter is available at:
  * https://github.com/mariusenglund/three-phase-inverter/tree/main/source-code
  *
  ******************************************************************************
  */


/* Calculate Timer Compare SV-PWM -------------------------------------------------*/
// Returns timer compare values using the Space Vector PWM algorithm.
compare_t calculate_timer_compare_svpwm(float Ud, float ma, uint32_t k_reload,
                                        uint32_t i1, uint32_t i2, uint32_t i3) {

  compare_t compare;
  float bias = k_reload;

  if (ma <= 1.0) { // Linear modulation
    float UAo1 = ma*(Ud/sqrt(3))*sine_table[i1];
    float UBo1 = ma*(Ud/sqrt(3))*sine_table[i2];
    float UCo1 = ma*(Ud/sqrt(3))*sine_table[i3];

    float Uk = (1/2.0)*(max(UAo1, UBo1, UCo1)+min(UAo1, UBo1, UCo1));

    compare.L1 = (uint32_t)(k_reload*((1/sqrt(3))*ma*sine_table[i1]-(Uk/Ud))+
                            bias/2.0);
    compare.L2 = (uint32_t)(k_reload*((1/sqrt(3))*ma*sine_table[i2]-(Uk/Ud))+
                            bias/2.0);
    compare.L3 = (uint32_t)(k_reload*((1/sqrt(3))*ma*sine_table[i3]-(Uk/Ud))+
                            bias/2.0);
  }

  return compare;
}
```

Code C.2: Microcontroller code for the Space Vector PWM algorithm (C).

C.3 Deviation Log MCU

Dev. No.	Date	Deviation	Solution
1	15 Apr 2023	Upon conducting PWM generation tests using an oscilloscope, it was discovered that the switching frequency observed was twice the expected value. While there could be multiple underlying causes for this, it is highly probable that it is attributed to inaccurate configuration of TIM1.	According to the documentation of the microcontroller, both the prescaler and auto reload parameter should be subtracted by a factor of 1. Refer to the code on GitHub for further details.
2	15 Apr 2023	There exists a discrepancy between the set and the actual frequency when using the SPWM technique. For instance, a set frequency of 50 Hz results in an output frequency of 48 Hz. The deviation varies with the resolution of the sinusoidal waveform.	A bug in the code resulted in the repetition of TIM1's initial and final compare values during a single time period (when the sinusoidal control signal transitions from 360 degrees to 0 degrees). A modification in the code logic was implemented to avoid calculation of the same compare value twice upon transitioning to a new time period.
3	17 Apr 2023	There appears to be a discrepancy in the output frequency of the sinusoidal waveforms when comparing SPWM and SV-PWM. It has been discovered that the microcontroller is unable to perform all necessary calculations rapidly enough when utilizing SV-PWM.	The program code has been optimized by utilizing lookup tables for sine values, instead of calculating them in real-time.
4	15 May 2023	A strange response was detected in the outputted PWM signal during testing when the amplitude modulation index was below 1.0. Upon troubleshooting, it was found that the compare values oscillated between 0 and ma*k_reload.	A revision of the program code was conducted wherein the bias was updated to be equal to half the value of the auto reload parameter. This modification ensures that the compare values now oscillate around k_reload/2.

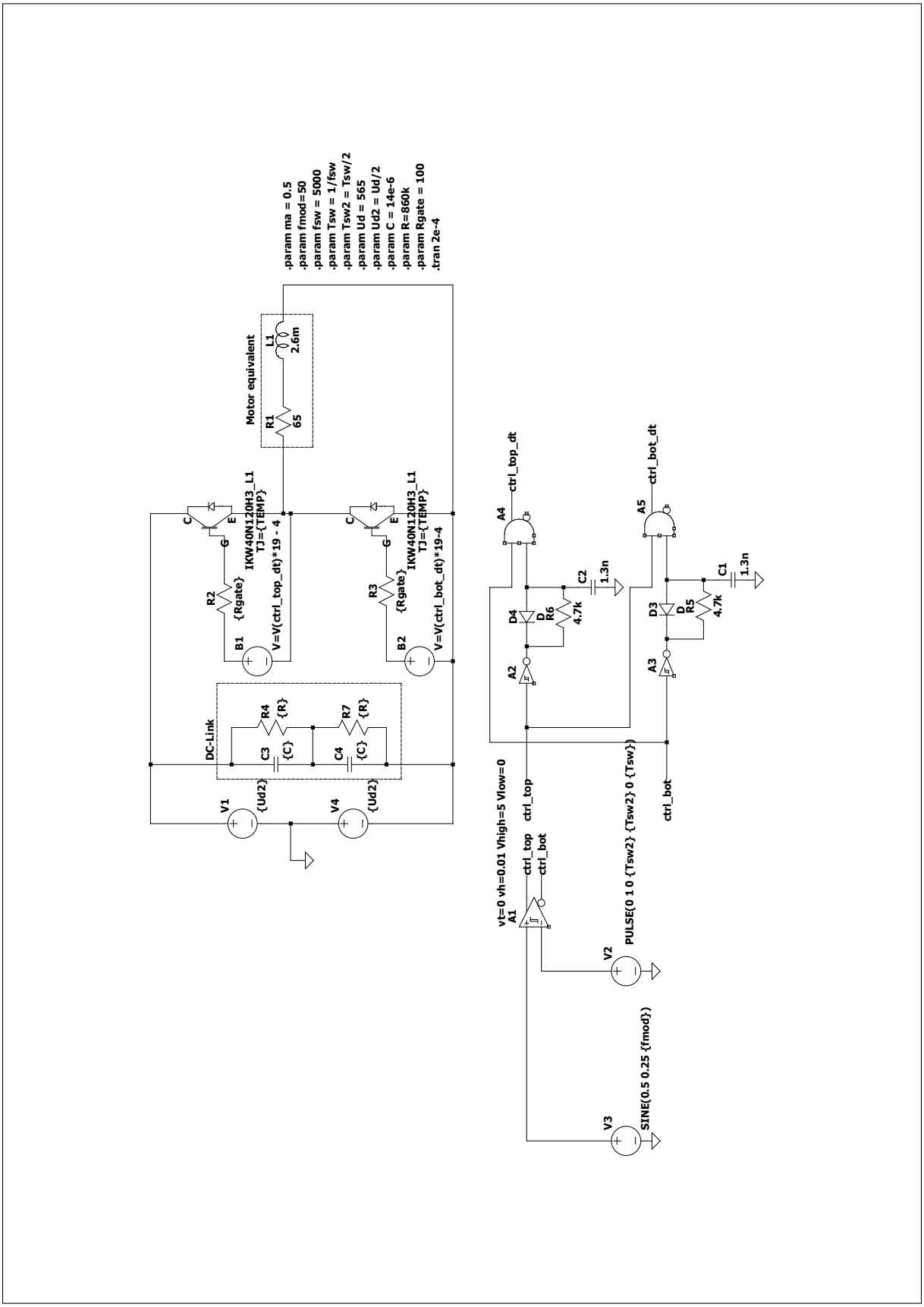
Appendix D

Simulation Results

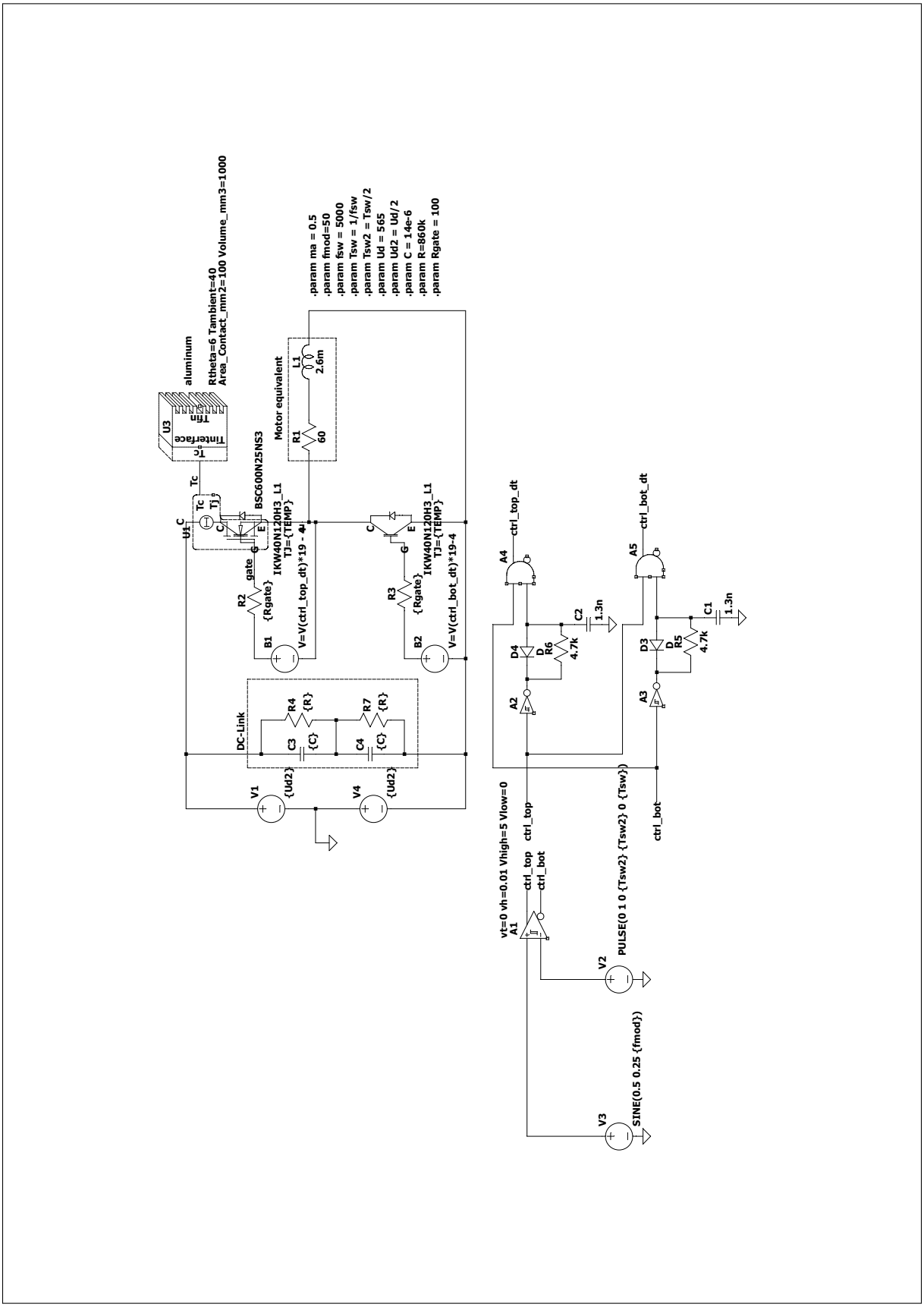
This appendix includes the results obtained from simulating the design with LTspice[1], along with code demonstrating calculation of the heat sinks.

[1] The LTspice project is available on GitHub

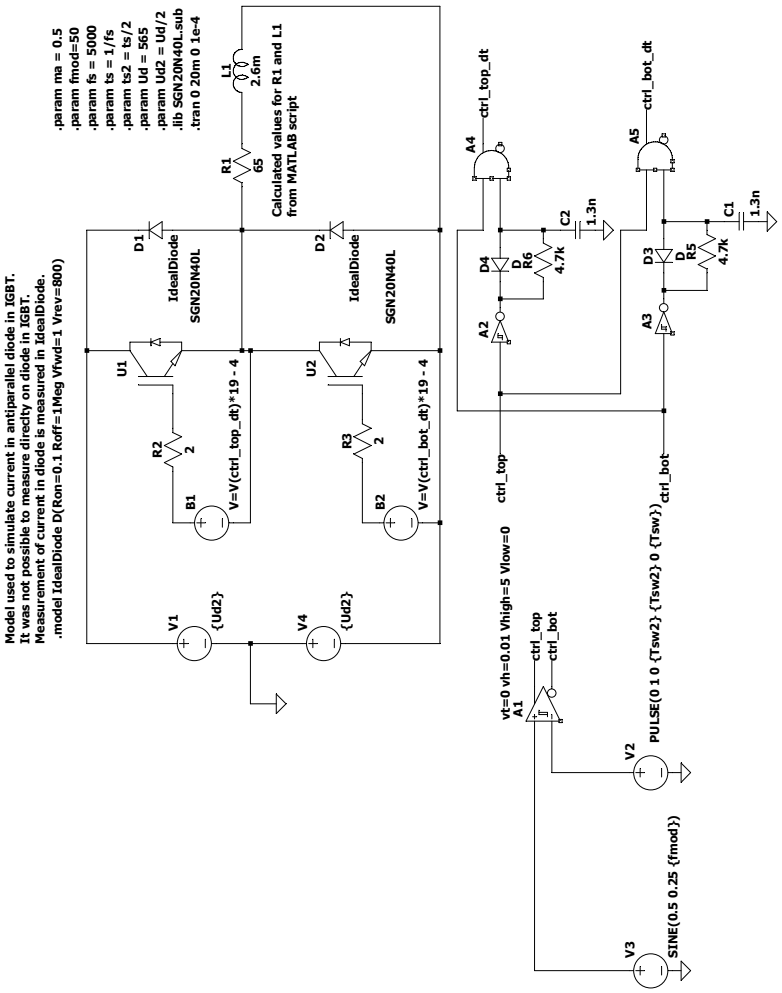
D.1 Simulation Model without Heat Sink



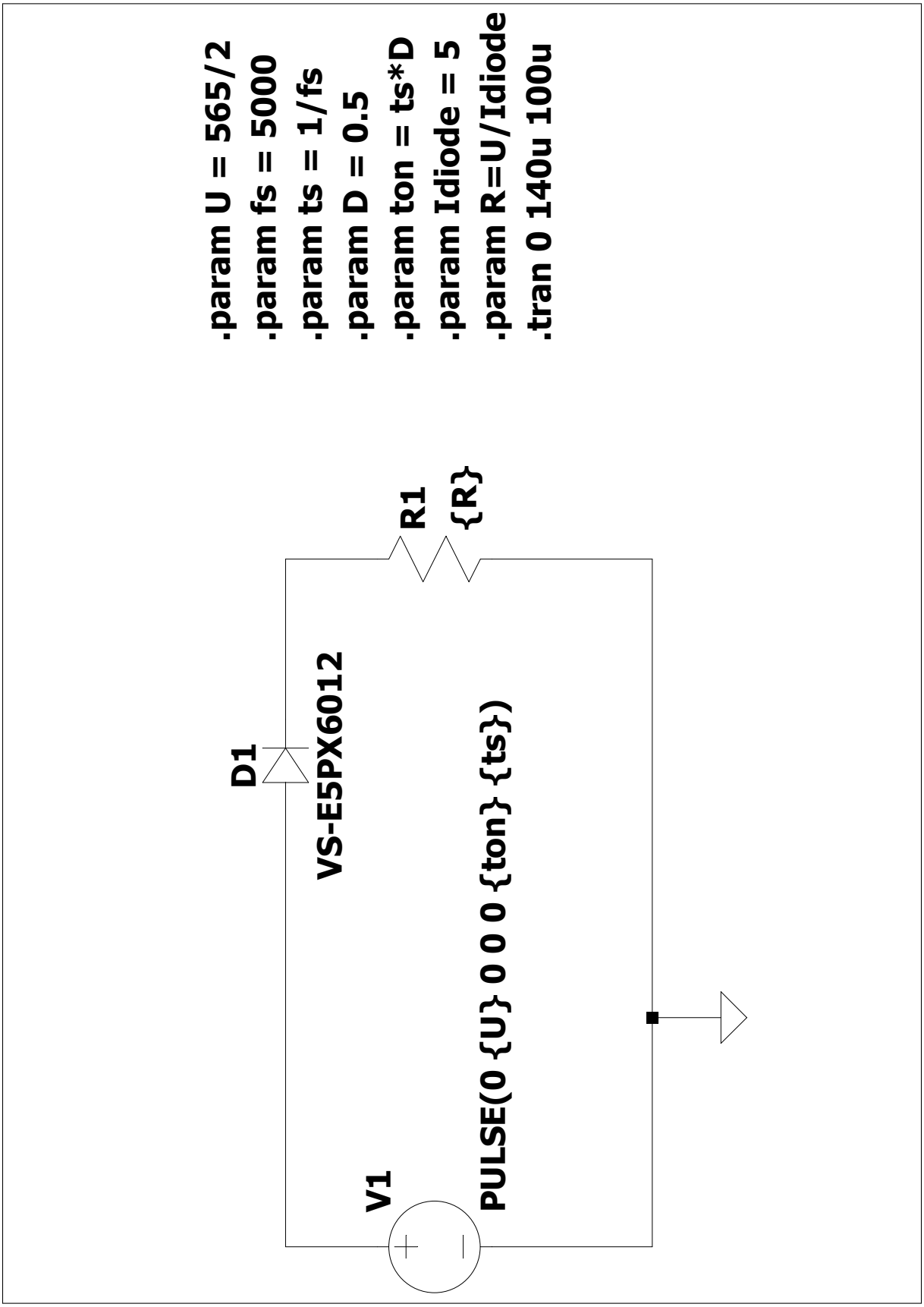
D.2 Simulation Model with Heat Sink



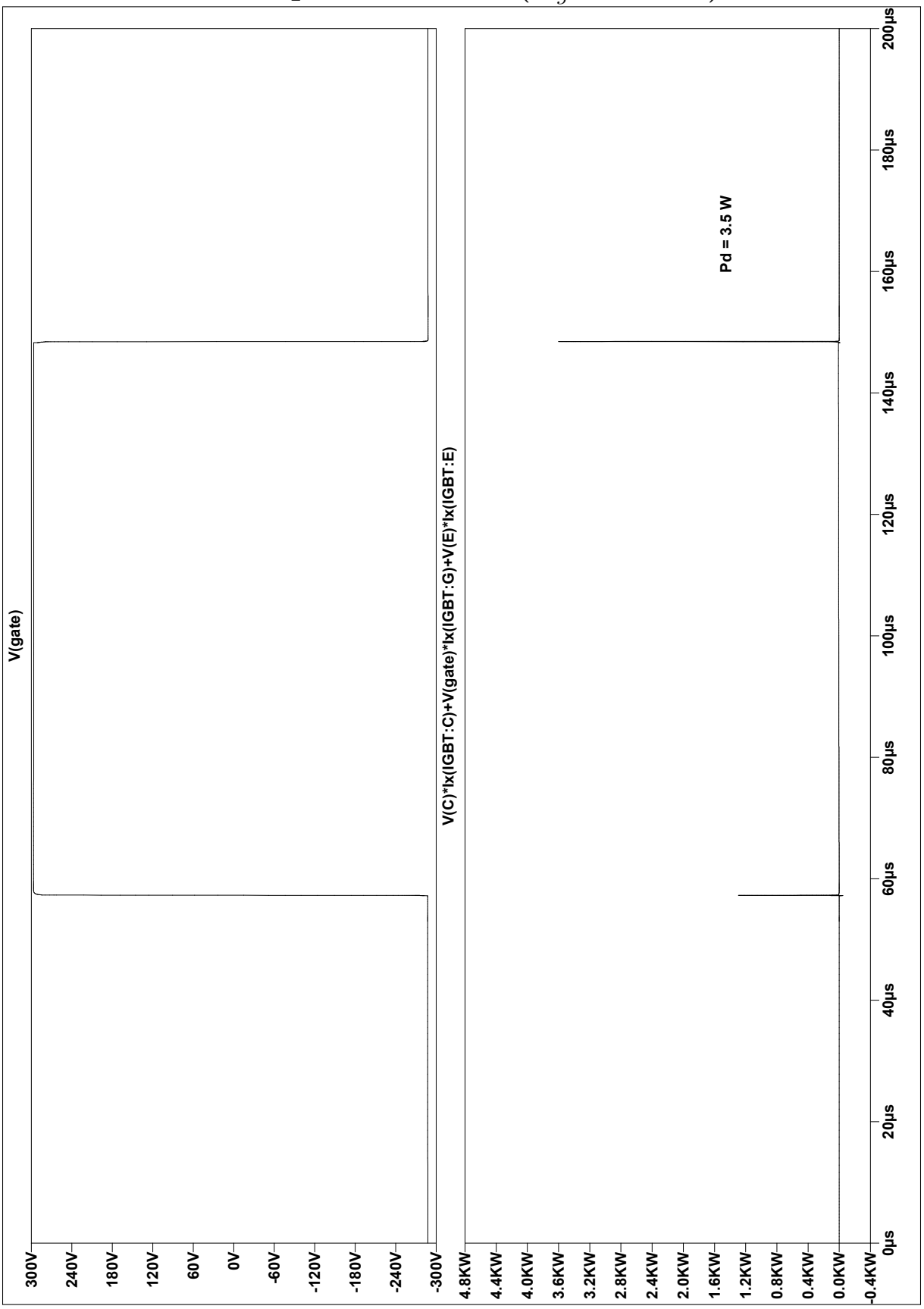
D.3 Diode Current Model



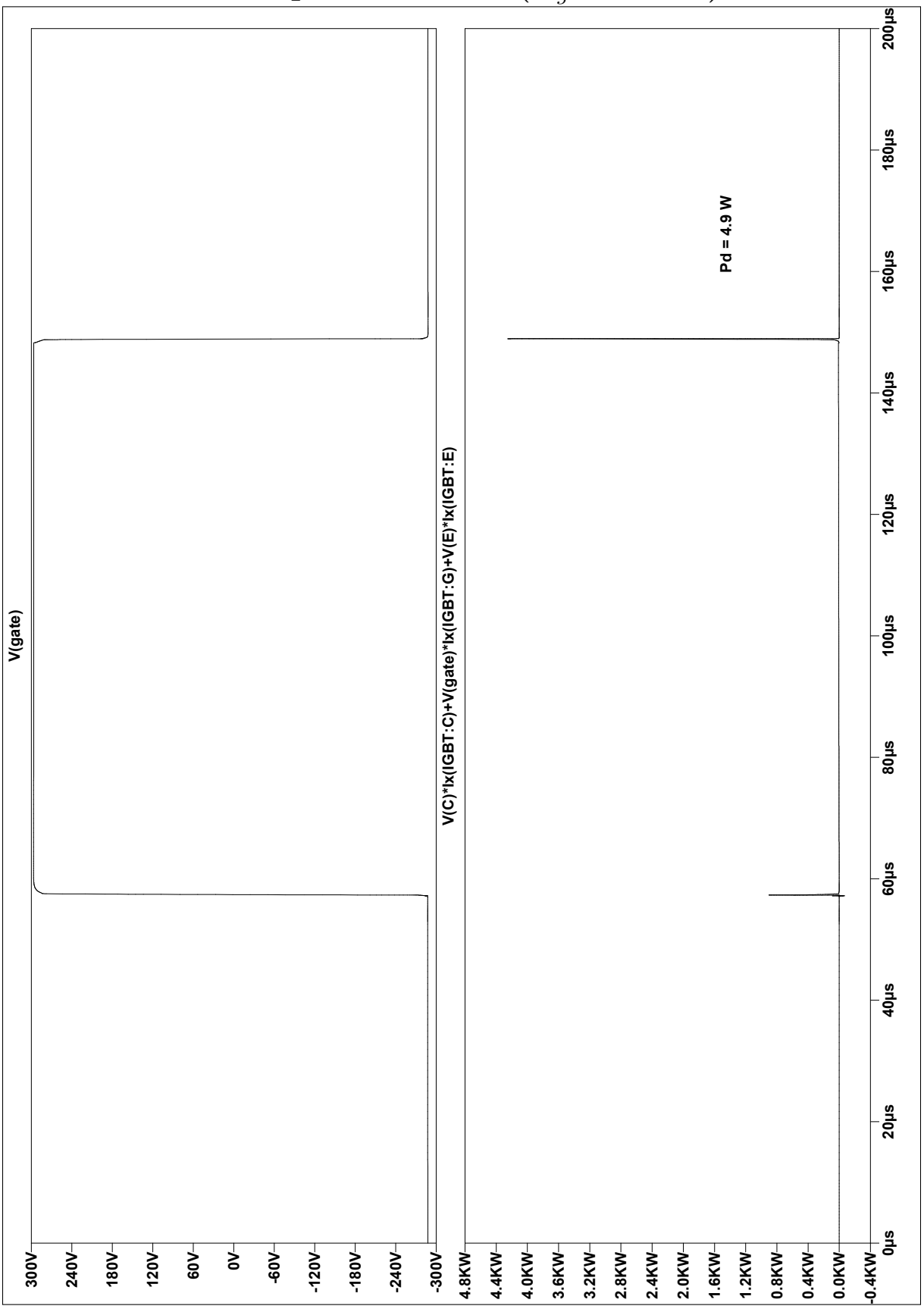
D.4 Reverse Recovery Diode Model



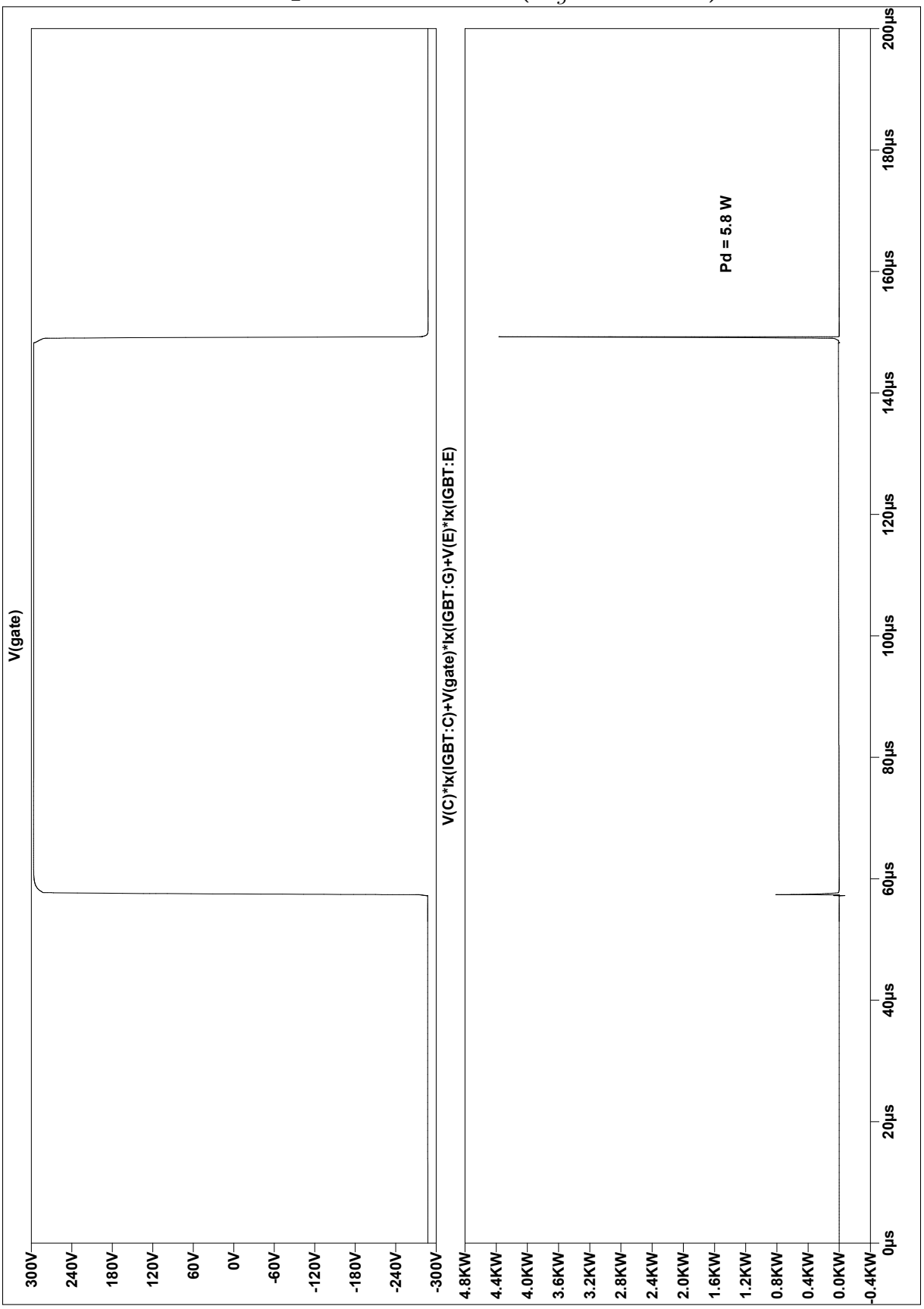
D.5 Power Dissipation IGBT ($R_{gate} = 12\,\Omega$)



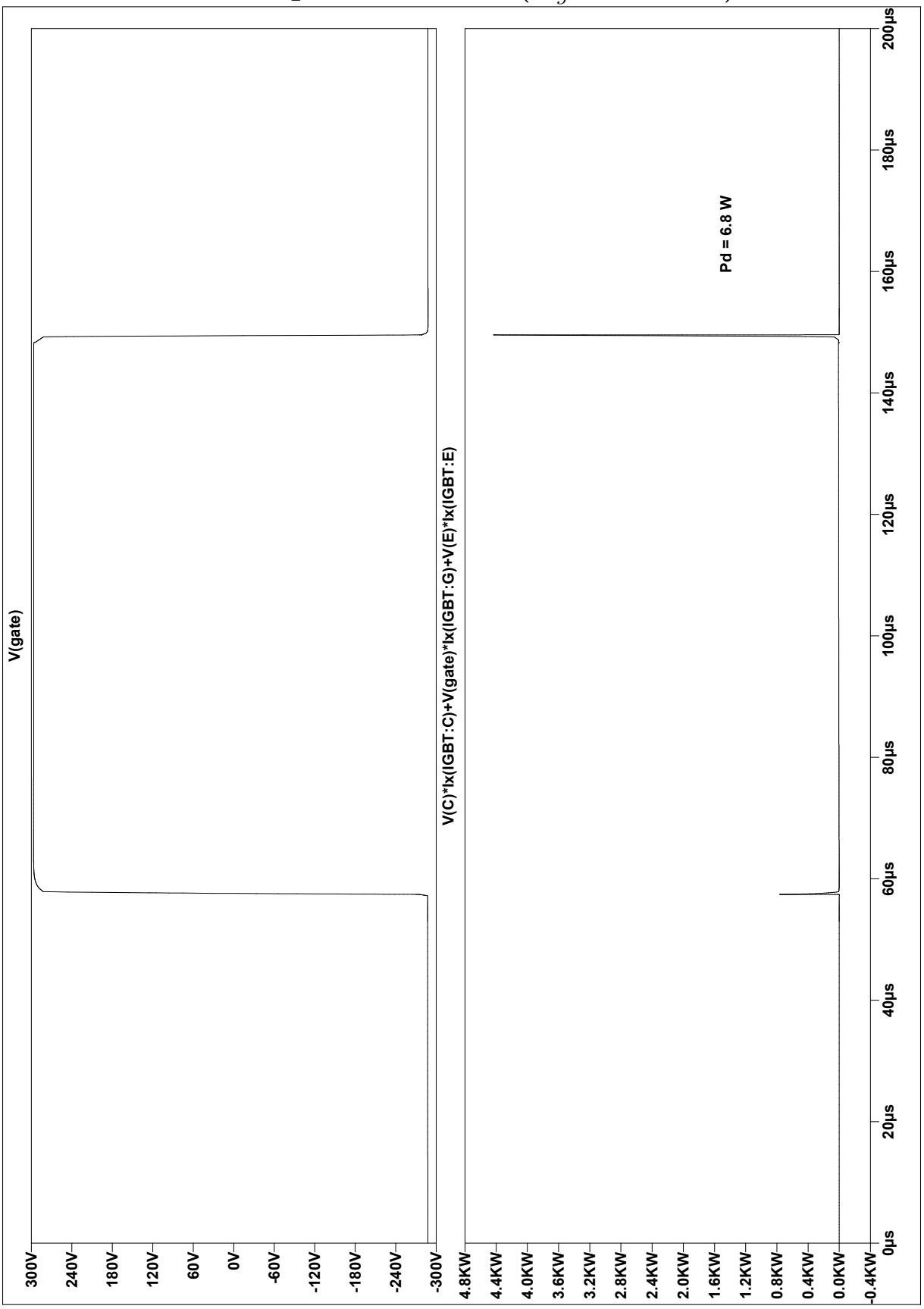
D.6 Power Dissipation IGBT ($R_{gate} = 50\,\Omega$)



D.7 Power Dissipation IGBT ($R_{gate} = 75\,\Omega$)



D.8 Power Dissipation IGBT ($R_{gate} = 100\,\Omega$)



D.9 Thermal Calculations

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
%   @brief          : Code for calculating power loss and size of heat sink for IGBT
%                     All values from IGBT datasheet IKW40N120H3
%   @author         : Marius Englund, Eirik Skorve Haugland, Ingrid Hovland
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


clc; clear; close all;

fs                      = 5000;   % operating switching frequency
U                       = 565;    % DC-link voltage
U_nom                   = 600;    % test condition voltage for IGBT, from datasheet
D                       = 0.5;    % duty cycle
Ts                      = 1/fs;   % switching period
td                      = Ts*D;   % dead time
Uce_sat                 = 1.8;    % @ 20 A
Ic                      = 5;      % operating @ 5 A
Ic_nom                  = 40;     % nominal current in datasheet
ma                      = 0.5;    % modulation index
cosfi                   = 0.7;    % typical cosfi for induction motor

%% Loss in diode
% calculating current through diode
Id_avg = (0.5+td/Ts)*(Ic/pi)-ma*cosfi*(Ic/8);
Id_RMS = sqrt((0.5+td/Ts)*((Ic^2)/4)-(ma*cosfi*(Ic^2)/(3*pi)));

% calculating E recovery in diode, values from datasheet
Qrr = 4.3e-6;   % charge from reverse recovery
Irm = 16;   % reverse recovery peak current
trr = 639e-9;   % reverse recovery time
Erec_nom = Irm*trr*U;   % reverse recovery energy diode @ I nominal

% finding on-state voltage and resistance for diode
delta_VD = 3.5-2.6;   % values from graph in datasheet
delta_ID = 70-30;
V_d0 = 1.35;
RD = delta_VD/delta_ID; % diode resistance

P_cond_diode = ((V_d0*Id_RMS)+(RD*(Id_RMS^2)))*D;   % conduction loss diode
P_sw_diode = (Erec_nom*fs*Ic*sqrt(2)*U)/(pi*Ic_nom*U_nom);  % switching loss diode
P_diode = P_sw_diode+P_cond_diode;  % total loss diode
fprintf("Switching loss diode = %.2f W\n",P_sw_diode)
fprintf("Conduction loss diode = %.2f W\n",P_cond_diode)

%%  Losses in IGBT
Ets = 1.3E-3;   % @ 175 degrees C and 5 A
P_cond_IGBT = Uce_sat*Ic*D;  % conduction loss IGHT
P_sw_IGBT = Ets*fs;   % switching loss IGBT
P_IGBT = P_sw_IGBT + P_cond_IGBT;   % total loss IGBT
fprintf("Switching loss transistor = %.2f W\n",P_sw_IGBT)
fprintf("Conduction loss transistor = %.2f W\n",P_cond_IGBT)
```

```
54
55 %% total loss in IGBT and diode
56 Pd = P_diode + P_IGBT;
57 fprintf("Total loss = %.2f W\n", Pd)
58
59 %% Thermal calculations
60 Tj = 175;   % junction temperature
61 Ta = 40;   % ambient temperature (worst case)
62 RthJA = 40;   % K/W junction-ambient without heatsink
63
64 % calculation of RthCS in PAD  (case-heatsink)
65 thermal_impedance_PAD = 0.107;  % from datasheet for pad  [K-in^2/W]
66 area_pad = 0.787^2;  % measurements from datasheet IGBT [in^2]
67 RthCS = thermal_impedance_PAD/area_pad;
68
69 % calculation of RthJC (junction-case)
70 RthJC_diode = 1.1;   % junction-case thermal resistance diode
71 RthJC_IGBT = 0.31;   % junction-case thermal resistance IGBT
72 RthJC = ((RthJC_IGBT*RthJC_diode)/(RthJC_IGBT+RthJC_diode));
73
74 % total thermal resistance
75 RthSA = (Tj-Ta)/Pd - (RthCS+RthJC);   % sink-ambient
76 fprintf("Total thermal resistance = %.2f K/W\n",RthSA)
77
78 %% calculate thermal resistance from dimensions of heat sink
79 % method from Power Electronics book, page 740-741
80 A1 = 0.01227;   % total area of heat sink in m^2
81 Fred = 0.7;     % distance between fins, from graph on page 742
82 dvert = 0.0038; % vertical measurement
83 deltaT = Tj-Ta;
84 RthDim = (1/(1.34*A1*Fred))*((dvert/deltaT)^(1/4));
85 fprintf("Thermal resistance of chosen heat sink = %.2f K/W\n",RthDim)
```

Code D.1: Script for thermal calculations (MATLAB).

Appendix E

Tools and Equipment

This appendix details the specific tools and equipment that were utilized in the implementation of the project.

E.1 List of Software Tools

Developer	Product	Version no.	Application
Microsoft	Teams	1.6.0	Project management
TeamGantt	TeamGantt	*online*	Project management
Massimo Redaelli	CircuiTikZ	1.6.1	Graphical contents
Lucid Software Inc.	Lucidchart	*online*	Graphical contents
Time Base Technology Limited	GoodNotes 5	5.9.90	Graphical contents
KiCad Developers Team	KiCad	6.0.9	PCB layout design
STMicroelectronics	STM32CubeIDE	1.12.0	MCU programming
Microsoft	Visual Studio Code	1.75.0	MCU programming
PlatformIO Labs	PlatformIO	6.1.6	MCU programming
Analog Devices	LTspice	17.1.6	Circuit simulations
National Instruments	Multisim	14.2.0	Circuit simulations
MathWorks	MATLAB	R2022b-1	General calculations

Table E.1: List of software tools that has been used throughout the project.

E.2 List of Laboratory Equipment

Equipment	Manufacturer	Model No.
Power Supply	TRI-OUTPUT	DF1731SL3A
Rectifier	EA Elektro-Automatik	EA-PS 9500-06 T
Load Resistor	*custom*	*custom*
Induction Motor	ABB Motors	M2VA71B-4
Oscilloscope	RIGOL TECHNOLOGIES	DS1054Z
Differential Probe	Micsig	DP10013
Current Probe	Micsig	CP2100A
Multimeter	AMPROBE	AM-520-EUR
Thermal Imaging Camera	FLUKE	Ti27

Table E.2: List of laboratory equipment utilized during the testing phase of the design.

Appendix F

Laboratory Exercise

This appendix comprises a laboratory exercise proposal that utilizes the inverter, intentionally developed as an educational resource to future laboratory experiments at Western Norway University of Applied Sciences. The objective of the exercise is to enable practical application of theoretical concepts by conducting measurements, performing calculations, and comparing the SV-PWM and SPWM techniques.

The exercise[1] is available on GitHub

[1] The exercise is founded on a template provided by the supervisor and is presented in the Norwegian language.

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Glossary

induction motor An electrical machine that converts electrical energy into mechanical energy.

inverter An electronic device or circuitry that converts DC to AC.

microcontroller A small computer on a single VLSI integrated circuit (IC) chip.

power processing unit A circuit device that converts the electrical voltage and frequency of the utility line into appropriate levels.

rectifier An electronic device or circuitry that converts AC to DC.

Acronyms

AC Alternating Current.

BJT Bipolar Junction Transistor.

DC Direct Current.
DTC Direct Torque Control.

EMI Electromagnetic Interference.

FOC Field Oriented Control.

IC Integrated Circuit.
IGBT Insulated-Gate Bipolar Transistor.

MCU Microcontroller Unit.
MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

ND Not Defined.

PCB Printed Circuit Board.
PPU Power Processing Unit.
PWM Pulse Width Modulation.

RMS Root Mean Square.

SPWM Sinusoidal Pulse Width Modulation.
SV-PWM Space Vector Pulse Width Modulation.

VFD Variable Frequency Drive.
VLSI Very Large Scale Integration.