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Simulations Of Busy Probabilities In The ALPIDE Chip And The Upgraded ALICE ITS Detector

S.V. Nesbo*[a], J. Alme[b], M. Bonora[e], P. Giubilato[c], H. Helstrup[a], S. Hristozkov[e], G. Aglieri Rinella[e], D. Röhrich[b], J. Schambach[d], R. Shahoyan[e], and K. Ullaland[b] for the ALICE ITS collaboration

[a] *Western Norway University of Applied Sciences, Norway*
[b] *University of Bergen, Norway*
[c] *Universita e INFN, Italy*
[d] *The University of Texas at Austin, United States of America*
[e] *European Organization for Nuclear Research (CERN), Switzerland*
E-mail: svn@hvl.no, johan.alme@uib.no, matthias.bonora@cern.ch, Piero.Giubilato@cern.ch, Havard.Helstrup@hvl.no, shristozkov@gmail.com, Gianluca.Aglieri.Rinella@cern.ch, Dieter.Rohrich@uib.no, jschamba@physics.utexas.edu, Ruben.Shahoyan@cern.ch, Kjetil.Ullaland@uib.no

For the Long Shutdown 2 (LS2) upgrade of the ITS detector in the ALICE experiment at the LHC, a novel pixel detector chip, the ALPIDE chip, has been developed. In the event of busy ALPIDE chips in the ITS detector, the readout electronics may need to take appropriate action to minimize loss of data.

This paper presents a lightweight, statistical simulation model for the ALPIDE chip and the upgraded ITS detector, developed using the SystemC framework. The purpose of the model is to quantify the probability of a busy condition and the data taking efficiency of the ALPIDE chips under various conditions, and to apply this knowledge during the development of the readout electronics and firmware.

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*Speaker.

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1. Introduction

For the ALICE LS2 upgrade at the CERN LHC in 2019-2020, a new Inner Tracking System (ITS) is under development. It is designed to be capable of operating at average event rates of up to 400 kHz in pp and 100 kHz in Pb-Pb, which represents a factor of 100 increase in event rates compared to the current ITS detector, and a factor two margin to the ALICE LS2 upgrade requirement [1].

A new monolithic pixel detector chip, the ALPIDE, has been developed to achieve this. Long, rectangular, arrays of ALPIDE chips, called "staves", will be organized in 7 circular layers to form the inner, middle and outer barrel of the new ITS, as seen in figure 1.

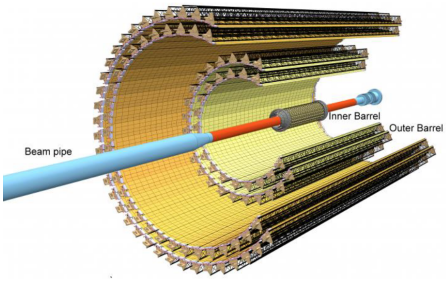

Figure 1: The upgraded ITS detector [1].

2. ALPIDE Busy Signaling

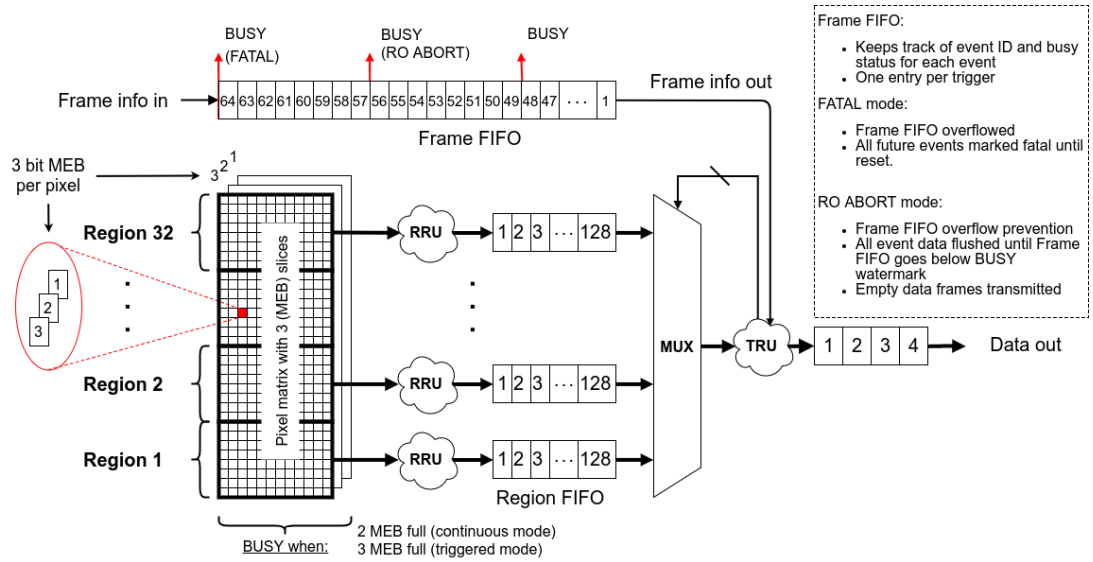

Figure 2: Simplified diagram of dataflow in ALPIDE chip, highlighting the event buffers, readout and framing.

To be able to process more than one event at a time, the ALPIDE chip incorporates a 3 bit deep Multi Event Buffer (MEB) in each pixel, as shown in figure 2. The pixel matrix is divided into 32 regions, and each region has a dedicated Region Readout Unit (RRU) which reads out data from the matrix. Data from the RRUs is read out and organized into event frames by the Top Readout Unit (TRU), and put on a FIFO for transmission off the chip. There is also a 64-word deep event framing FIFO, which means that the ALPIDE can in principle keep track of and process up to 64 events at the same time. [2]

Figure 3: Example of a serial data stream from the Alpide chip. The busy words have priority, and can appear at an arbitrary point in the stream, even in the middle of a data frame (the green data words).

A strobe signal is asserted when the chip receives a trigger. The length of the strobe is configurable, and when a hit coincides with the strobe window, the hit is latched into an event buffer. Two different modes of triggering and readout is supported by the chip; normal triggered mode, or continuous mode. In the triggered mode, the trigger is intended to come from an interaction trigger, and it is typically used with a short strobe window (on the order of a few hundred nanoseconds). In the continuous mode, the triggers are not based on interactions, but is generated periodically. Longer strobe windows will be used in this mode, typically around 10 microseconds long, and with a short gap of around 100 nanoseconds between each strobe. The chip can generate the triggers for the strobes internally in continuous mode, but external trigger can also be used.

Regardless of the mode of operation, each incoming triggered is honored with an entry in the event framing FIFO, which is used to encapsulate data into packages when it is sent off the chip, and to keep track of events.

The chip becomes busy if it runs out of MEB slices, or if the event framing FIFO goes above 48 events, as indicated in figure 2. The chip will then immediately output a BUSY_ON word on its data link, followed by BUSY_OFF when the busy condition goes away, as illustrated in figure 3.

3. Readout Electronics for the upgraded ITS

For each stave there is a Readout Unit (RU), which forwards incoming event data from the staves of ALPIDE chips on up to three optical GBT links, and is responsible for distributing synchronized triggers to all ALPIDEs [3].

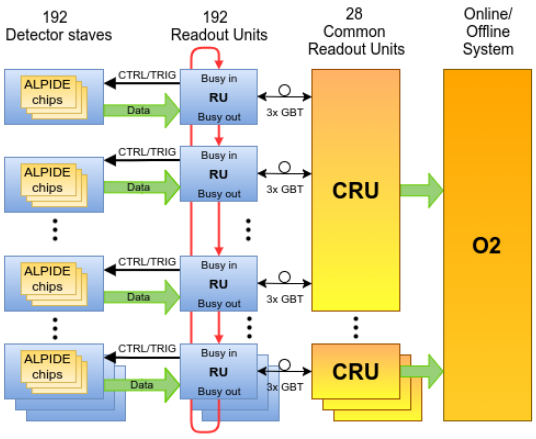

Figure 4: General overview of the readout system for the upgraded ITS detector. Busy daisy-chain between RUs in red.

Due to the random nature of particle collisions within bunch crossings, and despite of the highly parallel buffered architecture of the ALPIDE chip, there will inevitably be situations with high instantaneous event rates and/or high multiplicity events, where the detector will experience busy chips that are not able to cope with the amount of data. In those situations the RUs may be required to take active and coordinated measures across the detectors, to ensure maximum efficiency of the detector and prevent loss of data. The RUs have a port dedicated to signal BUSY information and they can be connected to facilitate this, such as in the daisy chain configuration in figure 4.

4. SystemC Simulation Model of ALPIDE and ITS

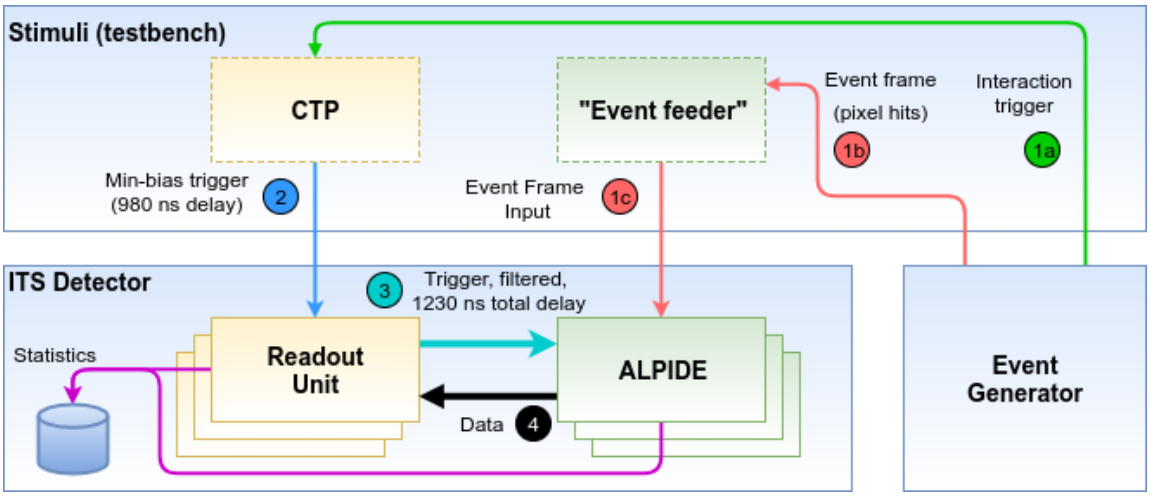

Figure 5: Overview of the SystemC simulation model for the upgraded ITS detector

In order to design a system for busy handling in the RU, and support specifications for the design of the data path in the firmware, a new simulation model of the upgraded ITS detector was developed using the SystemC framework, which is a C++ library for modeling digital circuits in a similar fashion to Hardware Description Languages (HDLs). The new model builds on some previous work done for the design of the ALPIDE internal readout circuits [4]. The digital readout logic of the ALPIDE chip is accurately modeled, since it is crucial for the simulation of busy situations. The main important components of the simulation model are shown in figure 5, where the general order of events in the simulation is indicated by the numbered bullets.

5. Event Generation and Data Input

The simulation comes with two modes for event input/generation. For more accurate simulations, Monte Carlo (MC) events are generated using the ITS upgrade ROOT macros from the aliRoot framework, based on what was done in a previous simulation model [4]. Adapting this approach to use real ALICE events can also be done. For high volume simulations, there is a mode with random hit generation, based on statistical distributions which can be modeled for an LHC experiment, such as the minimum-bias Pb-Pb distribution shown in figure 6.

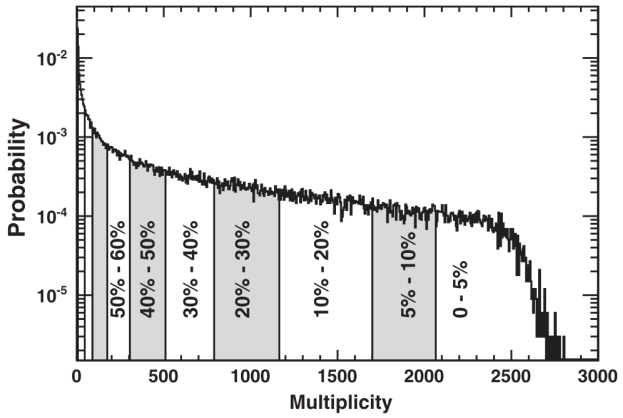

Figure 6: Uncorrected multiplicity distribution of charged particles in the TPC ($|\eta| < 0.8$) [5]

Inter-event times follow an exponential distribution in both modes. The statistical mode generates random events on the fly, and offers a faster (but less accurate) way to simulate a lot more events, increasing the chances of covering rare events with high multiplicity and high event-rates.

6. Results and outlook

Preliminary simulations for a single chip were run in triggered mode at different event rates, using the random hit generation mode with the minimum-bias Pb-Pb multiplicity distribution. The simulations were limited to the 3 innermost layers which have the highest expected hit densities. Previous single chip simulations that were run with a cycle-accurate Verilog model [6], using MC events with a hit density of $19.5\,\mathrm{cm}^{-2}$ and 100 kHz event rate, yielded an efficiency of $(99.84 \pm 0.03)\,\%$.

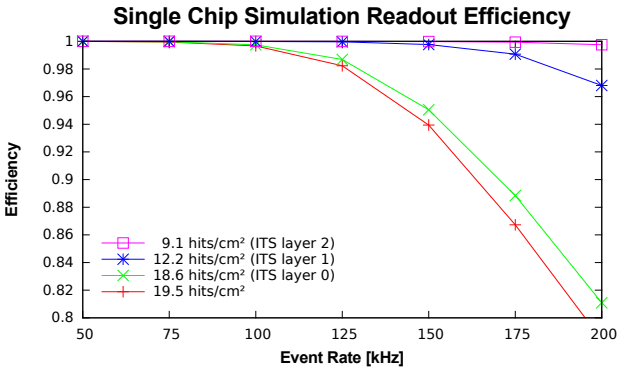

Figure 7: Pb-Pb efficiency simulations using the statistical event generator, with hit densities corresponding to those expected in the 3 innermost ITS layers at mid-rapidity [1], and hit density used in cycle-accurate Verilog simulations.

Figure 7 also includes a set of simulations with this hit density, where an efficiency of $(99.660 \pm 0.002)\,\%$ was obtained at 100 kHz, which is relatively close to the number obtained with the cycle-accurate model, considering that it was run with completely different input events. Readout efficiency is here defined as $100\% \times \frac{\text{Number of accepted triggers}}{\text{Total number of triggers}}$.
The results in figure 7 also show good correspondence with readout efficiency estimations that were done before the number of MEBs in the ALPIDE was specified [7]. As expected, the upgraded ITS has a high efficiency for the event rates it is designed to operate at, i.e. doing the busy handling locally at the RU-level may prove sufficient. Future simulations of the whole detector and readout chain will answer these questions by providing important data about detector efficiency, as well as allowing for benchmarking of busy handling solutions that are currently under development.

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