Radiation-Tolerant, SRAM-FPGA Based Trigger and Readout Electronics for the ALICE Experiment

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***Abstract*—The ALICE detector is a dedicated heavy-ion detector at the Large Hadron Collider which is commissioned end of 2007 at CERN. The ALICE triggers are handled by the Central Trigger Processor and distributed to all sub-detectors, amongst other the Time Projection Chamber and the Photon Spectrometer. The Front End Electronics of the Time Projection Chamber and the Photon Spectrometer share many of the same components. The Photon Spectrometer provides the trigger system with level 0 and level 1 triggers (e.g., high-p_t photons) by the use of several Trigger Router Units and a Trigger-OR board. The trigger electronics and the Front End Electronics are situated close to the collision-point, and errors due to radiation effects are to be expected.**

This article will give an overview of the trigger system from trigger generation with the Photon Spectrometer to trigger reception of the Front End Electronics of both detectors. How to deal with the possible effects of the radiation environment on the electronics that do trigger handling will be evaluated.

***Index Terms*—Detectors, radiation environment, readout electronics, trigger systems.**

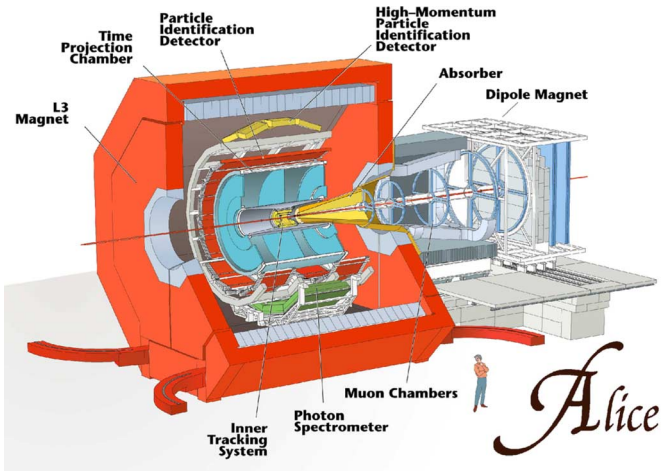

Fig. 1. The ALICE detector. The scale of the detector is given by the person standing next to it.

I. Introduction

THE ALICE (A Large Ion Collider Experiment) detector [1] is currently under commissioning as one of the experiments using the Large Hadron Collider at CERN. The Large Hadron Collider is a circular particle accelerator, where bunches of particles are accelerated to a beam energy of 5.5 TeV per nucleon for lead nuclei beams and 7 TeV for proton beams and then collided. The produced particles from these collisions are measured by the different experiments. The ALICE experiment is primarily designed to take measurements from Pb-Pb collisions, but will also investigate p-p events.

The ALICE detector (Fig. 1) consists of several sub-detectors with the purpose of recording high multiplicity events. The event rate for Pb-Pb collisions at the LHC maximum luminosity of 10^{27} $cm^{-2}s^{-1}$ will be about 8000 minimum-bias collisions per second. This low interaction rate makes it possible for ALICE to use slow but high-granularity detectors, such as the time-projection chamber (TPC) and the silicon drift detectors. A trigger based data readout system is designed to cope with such complicated events and a detector set that varies in both sensitive period and readout time. There are two major types of triggers in ALICE; the hardware triggers and the High Level Trigger. The hardware triggers reduces the overall data-rate to about 25 GB/s, while only 1.25 GB/s is stored to disk after the fast online data analysis provided by High Level Trigger. As the High Level Trigger is a separate system from the hardware trigger, this article will focus only on the latter. The Central Trigger Processor (CTP) generates three types of hardware triggers: calibration triggers, software triggers and physics triggers. The physics triggers are based on information coming from different trigger detectors, of which the PHOton Spectrometer (PHOS) is one. The different triggers are distributed by the CTP [2] to the sub detectors.

Major parts of the Front End Electronics (FEE) are common for PHOS and TPC. All sub-detectors initiate a readout sequence when triggers are received. Since the FEE is situated

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in a radiation environment and make use of commercial off-the-shelf SRAM-based FPGAs, radiation induced functional errors are a major concern. To reduce the possibility of such errors to occur in the trigger path, the logic for trigger reception is located in the same FPGA as is used for the data flow. This FPGA is a Xilinx Virtex-II pro [3]. The Xilinx Virtex-II pro supports a feature called Active Partial Reconfiguration, which can be used to correct single event upsets (SEUs) in the configuration memory of the FPGA.

II. Front End Electronics and Trigger System

A. Time Projection Chamber

The TPC detector, which is the main tracking detector of ALICE, is surrounding the beam pipe as shown in Fig. 1. The TPC barrel is a closed environment filled with gas. An applied electric field makes the secondary electrons drift in the gas volume towards the readout chambers at the end-caps on each side of the barrel. In the readout chambers the charge is amplified and collected by a 2-dimensional readout system. Together with the drift time this provides 3-dimensional spatial information. The FEE is located directly behind the end-caps. The two end-caps are divided into 18 sectors each, all in all serving roughly 560000 individual data-channels that are read out by 4356 Front End Cards (FECs) connected to 216 Readout Control Units (RCUs). More information on the Front End Electronics components and architecture can be found in [4].

B. Photon Spectrometer

The PHOS detector is one of the outermost detectors in Fig. 1. It measures electromagnetic showers of up to 100 GeV via a large matrix of $PbWO_4$ crystals, each read out by an avalanche photodiode. 32 crystals are connected to one FEC, and there are 28 FECs connected to one RCU via two separate readout branches. Each branch matches a crystal mapping of 16×28 crystals. There are 4 RCUs per PHOS module. In the initial run there will only be one PHOS module present, but in the final configuration there will be five modules, with an angular coverage of $5 * 20$ degrees. The pseudo rapidity coverage is -0.12 to 0.12.

PHOS is also a trigger detector. In addition to the FECs there is one Trigger Router Unit (TRU) card connected to each branch of 14 FECs defining a trigger region. Each FEC in a trigger region submits analogue sums of the input signals to the TRU. These analogue sums are digitized and then processed by the FPGA on the TRU into level 0 and level 1 triggers. The Trigger-OR board combines triggers from all TRUs, and forwards them to the CTP.

C. The Readout Control Unit (RCU)

Both in TPC and PHOS a Readout Control Unit (RCU) is used to control the data readout (see Fig. 2). The RCU is built up of an RCU motherboard, a Detector Control System (DCS) board and a Source Interface Unit card. The RCU motherboard is connected to the FECs via two branches. The front-end part of the FECs is different for the two detectors, but they share the same interface to the RCU. On both types of FECs, a set of

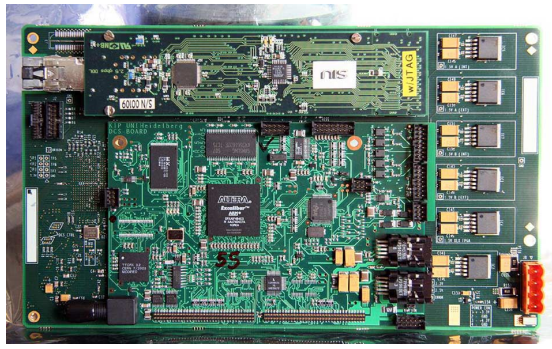

Fig. 2. The readout control unit. The RCU motherboard is in the back with the SIU card (top) and the DCS-board (bottom) attached.

mixed mode ASICs called ALTROs [5] are used to do analog to digital conversion, low level processing, and sampling and buffering of the data. The Source Interface Unit card ships the data to the DAQ system using an optical connection.

The DCS board is used for configuration and control of the FEE. The board is an embedded computer including an Altera FPGA with an ARM processor core, SRAM and a flash device acting as a hard drive. The DCS board is running a lightweight version of Linux, and communication to the upper layers of the DCS is done via Ethernet. In addition it connects the FEE to the local Trigger, Timing and Control (TTC) system via the TTC receiver chip (TTCrx). The TTCrx chip is connected to the Altera FPGA on the DCS board. In addition, two lines—L1 accept line and serial B channel, are routed from the DCS board to the FPGA on the RCU board.

D. PHOS as a Trigger Detector

Since the PHOS detector is designed for detecting photons, it is fast enough to be used for level 0 (L0) and level 1 accept (L1a) trigger decisions in ALICE (see Fig. 3). The timing requirements for generating the L0 trigger are very tight. PHOS must deliver the L0 trigger to the CTP 800 ns after the time of interaction. This includes the extra delay of 200 ns given by the cable length from the Trigger-OR to the CTP of 40 meters. The L0 and the L1a trigger is based on 8 analogue sums per FEC, performed on the FEC by fast summing shapers over a 2×2 crystal matrix, before being fed to the TRU.

1) Trigger Router Unit (TRU): The present version of the TRU contains a Xilinx Virtex-II pro FPGA. 14 analog-to-digital converters digitize the 112 analogue input signals received from the FECs, before entering the FPGA. The triggers are generated in the FPGA by summing up 2×2 analogue sums giving a total area of 4×4 crystals in space, and additionally summing up the analogue input signals in time over a time span of 100 ns. The L0 trigger is issued if the deposited energy given by the space-time sum exceeds a programmable threshold between 10 and 230 MeV. Three L1a triggers can be issued if there has been a valid L0 decision. These are based on three different programmable thresholds between 0.5 and 30 GeV. The thresholds are based on the value of transverse momentum of the photon: high p_t, mid p_t and low p_t. The TRU is presented in [6] and the firmware solution is discussed in depth in [7].

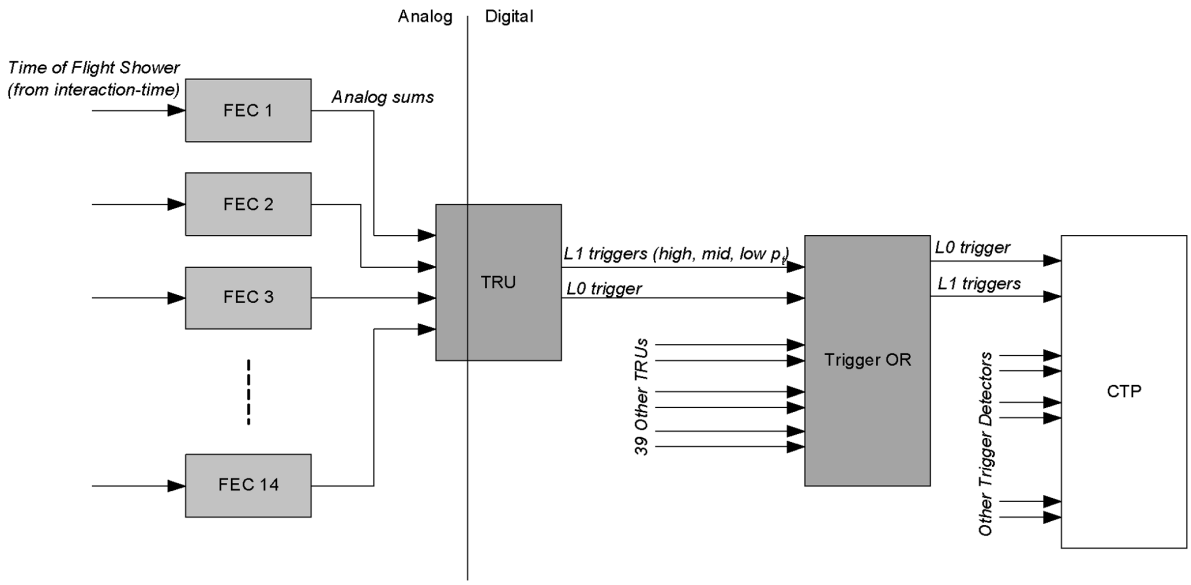

Fig. 3. PHOS used as a trigger detector. One trigger region is shown. From the time of interaction to the generated level 0 trigger reaches the CTP, not more than 800 ns must pass.

As the TRU is a part of the PHOS FEE it is located in the radiation environment. Functional errors in the FPGA are expected, and the same solution as given in Chapter IV is used on this board. The only difference is that communication to the Active Partial Reconfiguration device is done via an I2C interface on the RCU backplane.

2) Trigger-OR: The Trigger-OR board is equipped with a Xilinx Virtex-4 FPGA. The purpose of the Trigger-OR board is to gather all the L0 and L1a triggers coming from the altogether 40 TRUs in the PHOS detector. The L0 triggers are ORed through a fast OR gate. The same approach is currently used for the different L1a triggers as well.

The present concept of the TRU analyzing the data, while the Trigger-OR only forwards the triggers to the CTP will be changed in the future. The raw data will be shipped from the TRU to the Trigger-OR, leaving the data analysis to the latter. This opens the possibility to treat the PHOS detector as a whole, not being limited by the boundaries of a trigger region.

The Trigger-OR is in the same radiation environment as the FEE. There is no Active Partial Reconfiguration network on the Trigger-OR board, but doing Active Partial Reconfiguration as described in Chapter IV is possible from the DCS board. This is taken care of by a Linux kernel module that has direct communication with the configuration interface of the FPGA. Dedicated software for reconfiguration can run in parallel with the other tasks of the DCS board.

E. Trigger System Overview

A data readout sequence is only initiated when an indication of an actual event is detected. In Fig. 4 this is exemplified by the PHOS detector. PHOS is one out of twenty-four sources for the L0 and L1a triggers that the CTP uses for evaluation. The different trigger sources are ANDed together in the CTP since it was found that the ALICE triggers does not require that complex logic [8].

The CTP distribute the triggers and associated information such as event ID to local TTC systems for each sub-detector. The TTC forwards these data to the FEE via an optical line. The ALTRO is continuously sampling the data, and in PHOS, an L0 trigger from the CTP tells the FEE to start to buffer data with a configurable number of pre-samples. The TPC, which is a much slower detector, will start to buffer data on arrival of the L1a trigger. The CTP sends messages that can be decoded by the FEE to level 2 accept triggers. Then the RCU will try to ship the data to the Data Acquisition (DAQ) system, represented by the Data ReadOut Receiver Cards (D-RORCs) in Fig. 4. The FEE has the ability to buffer 4 or 8 events depending on configuration, so if the DAQ system is busy, the event will be shipped whenever possible.

In parallel with the FEE a BusyBox device is doing busy handling. The BusyBox receives the same events from the CTP as the FEE does. In addition it polls the D-RORCs for the latest events received. This information combined is used by the BusyBox to know when the buffers on the FEE are full. If so, the BusyBox tells the CTP that is should stop sending triggers until the buffers in the FEE are available. The Trigger Receiver Module that decodes the trigger information from the CTP is common for the TPC and PHOS RCU and for the BusyBox.

The vertical line in Fig. 4 divides the devices that are located on the detector side from those that are located in the counting room. All devices on the detector side are in the radiation environment, while those in the counting room are operating under normal conditions.

III. Trigger Handling

A. Trigger Generation

The CTP receives and distributes the triggers to the ALICE detector. The triggers are hierarchically divided into three levels. The L0 trigger is the fastest trigger with a latency of 1.2 μs from the time of interaction. The L1a trigger has a latency of 6.5 μs,

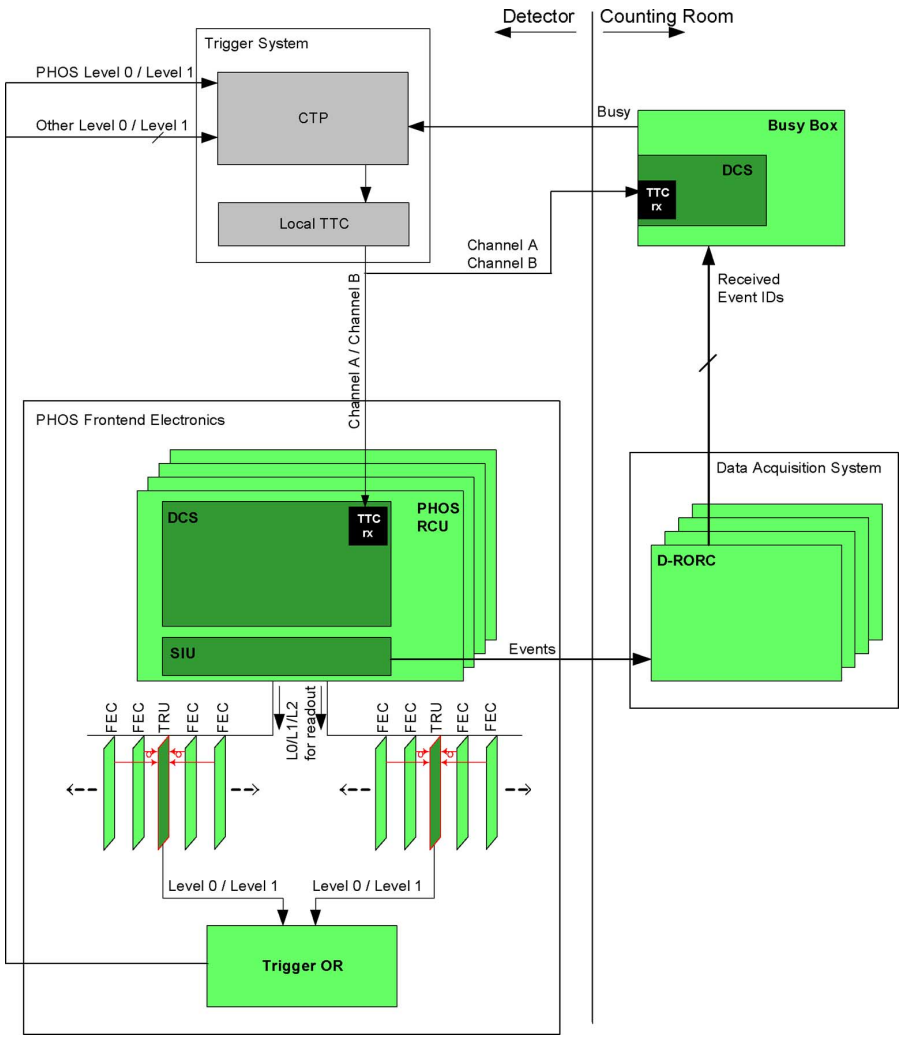

Fig. 4. Sketch of the trigger system for PHOS detector that shows how PHOS acts as a trigger detector as well as how PHOS uses triggers generated by CTP for data readout.

while the level 2 (L2) trigger has a latency of approximately 88 μs. L0 and L1a are generated based on information that is received by the CTP within the L0 latency and the L1a latency respectively. The very late L2 is decided by the past-future protection condition. The purpose of this is to make sure that pile-ups comprising the data are avoided within a programmable time-interval before and after the collision. Under normal operation this time is decided by the drift-time of the TPC detector.

The FEE receives the trigger information from the local TTC system in two channels. Channel A (named L1 accept line on the FEE) submits the L0 and the L1a as pulses of different length. On serial channel B accompanied information concerning the L1a trigger is sent by an L1a message. The L2 trigger is only submitted as a message on serial channel B. This can either be an L2 accept message or an L2 reject message, depending on whether the past-future protection condition has been violated or not.

A possible future add-on is the Region of Interest feature. This enables the FEE to only read out parts of the sub-detectors. If included the Region of Interest information will be sent on serial channel B, but since it is still not implemented it will not be given any attention in this article.

1) Trigger Sequences: The triggers generated by the CTP are divided into physics triggers, calibration triggers and software triggers. A legal sequence of triggers and messages for physics triggers and software triggers are defined to be L0—L1a—L1a message—L2a/L2r message. Software triggers are used to give information to the FEE and the DAQ system. Two software trigger sequences have been defined so far; start of run and end of run. A calibration trigger sequence is always started by a pre-pulse. Apart from the pre-pulse, the calibration sequence is identical to the other sequences.

2) Serial Channel B Messages: There are two types of messages transmitted on serial channel B: individually addressed messages and broadcast messages. The first ones are used to submit L1a and L2 trigger information. The broadcast messages are event-counter reset, bunch-crossing-counter reset and calibration pre-pulse. Additional broadcast messages might be added in the future.

Broadcast messages are composed of one single word, while addressed messages are divided into several words with a header word followed by data words. Some of the information in the L1a message and the L2 message is identical. This allows the receiver to verify that the messages belong to the same event. The

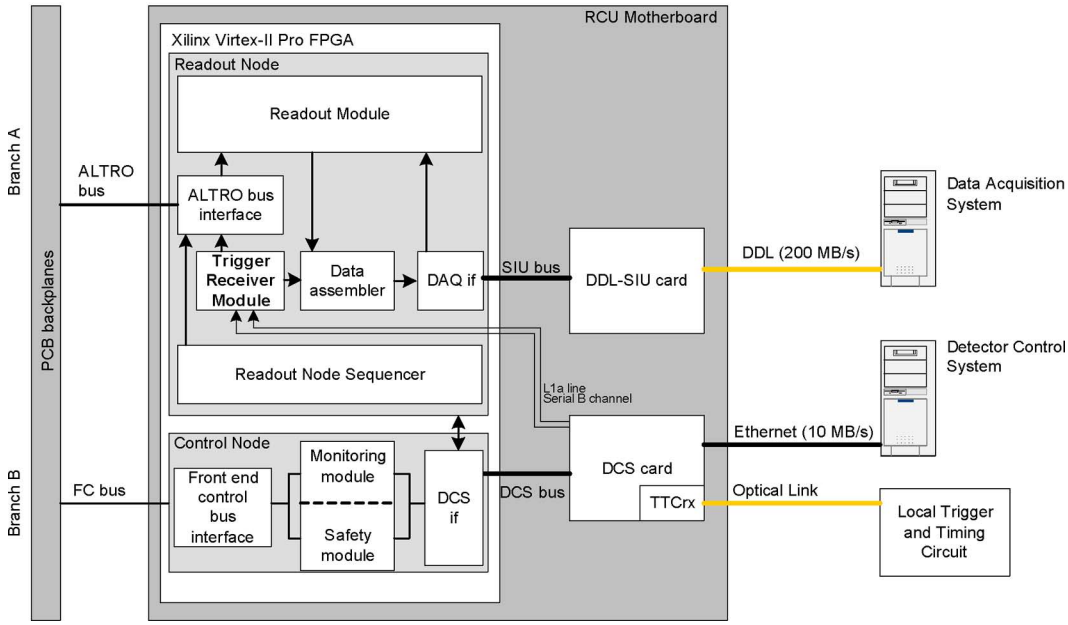

Fig. 5. Conceptual sketch of the RCU Xilinx firmware put into context.

level 1 message header word contains information on whether it is a calibration trigger, a software trigger, the type of the calibration trigger and whether a Region of Interest message is to be expected. The rest of the information in the level 1 message is devoted to trigger class. The trigger class is defined by the set of trigger inputs, which sub-detectors are participating in the event, rare/non-rare classification, past/future requirements and a few other control bits.

The L2 accept message consist of one header word and seven data words. The header word is the bunch-crossing ID. There are 3564 bunches of particles in one orbit, and the bunch-crossing ID is the number of the two bunches that participated in the event. A FEE local bunch-crossing ID can be generated by counting the clock, since the frequency of the bunch-crossings is the source of the system clock. The FEE local bunch-crossing ID is decided to be sampled when the L1a trigger arrives, and it is used for verifying the received bunch-crossing ID. L2 accept message data words 2 and 3 contains orbit ID. This is a counter counting the number of times all bunches has orbited. The orbit ID and the bunch-crossing ID is the information needed to completely identify an event. Data word 4 contains information on trigger cluster, whether it is a calibration trigger, software trigger and whether a Region of Interest message should have been included in the event sequence. The rest of the L2 accept message contains trigger class for a physics trigger, while for a software trigger, it contains information on the participating sub-detectors. The L2 reject message is only a header word containing the bunch-crossing ID.

B. PHOS and TPC Trigger Reception

1) Overview: When the trigger information reaches the FEE via the optical fiber, it is decoded by the TTCrx on the DCS board. The TTCrx has a register interface towards the Altera FPGA. It forwards the global system clock, as well as the information arriving on channel A (named L1 Accept line on the FEE) and serial channel B. For PHOS and TPC the trigger decoding feature in the TTCrx is not used. The main reason is that the Altera FPGA on the DCS board is sensitive to SEUs. Additionally the TTCrx has no support for decoding L0 triggers.

With this in mind, it has been decided to do trigger decoding on the RCU motherboard. The L1 accept line and the serial channel B are available for the Xilinx Virtex-II pro FPGA. This FPGA is sensitive to SEUs at approximately the same rate as the Altera FPGA on the DCS board [9], but the Active Partial Reconfiguration will increase the radiation tolerance to an acceptable level.

2) RCU Firmware: The RCU firmware has two main tasks; Data readout and low level control system functionality [10]. In Fig. 5 these main tasks are divided into a readout node and a control node. The control node is used for monitoring critical values on the FECs such as voltage levels and temperatures. Since a readout sequence is initiated by the reception of triggers, the Trigger Receiver Module is placed in the readout node. An L2 accept trigger will freeze the latest event data and store it in the ALTRO data buffer. The second phase of the data readout is to push the data to the DAQ system. The given event is then read out channel by channel and buffered in the RCU. In the Data Assembler module the ALTRO data are wrapped with 8 header words and one trailer word to match the ALICE DDL data format; the Common Data Header (CDH) [11]. Except for some information regarding block size and error/status, all information in the CDH is extracted by the Trigger Receiver Module from the data being sent the CTP.

3) Trigger Receiver Module: The RCU Trigger Receiver Module (see Fig. 6) interfaces the local TTC system on the FEE. Both the serial channel B and the L1 accept line is synchronous with the system clock. All messages that are being transmitted via serial channel B are hamming coded.

The Trigger Receiver Module consists of several sub-modules with different tasks. The L1a trigger line decoder decodes

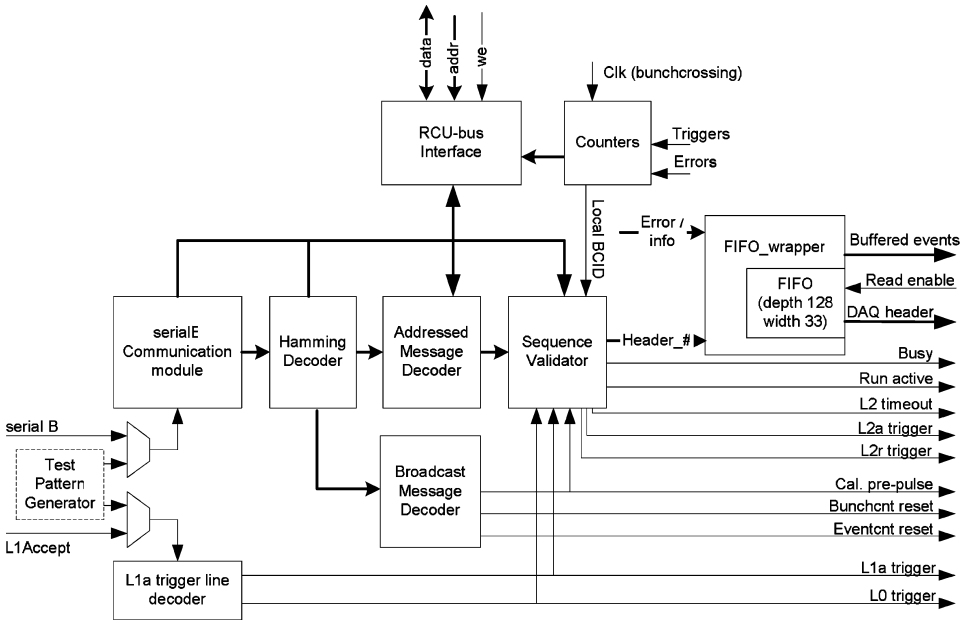

Fig. 6. Schematic overview of the trigger receiver module.

L0 and L1a triggers. The serial B communication module decodes messages received on the serial channel B. When completely received, the messages are hamming decoded before being analyzed by the addressed message decoder. This sub-module evaluates all the addresses received and buffers the data in register arrays matching the various messages. The counter sub-module includes counters for bunch-crossing, errors and received triggers and messages. In addition it sets up the time-windows based on the programmable latencies for when the different triggers are to be expected in time. The sequence validator verifies the trigger sequence. Any error concerning missing triggers, timeouts and content errors are reported. In addition the sequence validator decodes calibration and software trigger sequences.

The Trigger Receiver Module is in a busy state until a sequence has been completely received, i.e., until a valid L2 trigger has been decoded or there has been an L2 timeout condition. The data is then formatted to match the CDH format and stored in a FIFO together with two words containing event-status and event-error. The FIFO is able to store more than 8 events, which is decided by the number of buffers in the ALTRO. The event-status word and the event-error word have more detailed information than what is space for in the CDH. The FIFO has optional parity encoding. All events, including software events, calibration events, rejected events and erroneous events are stored. The FIFO is to be read out internally in the RCU firmware by the data assembler. Technical documentation for the Trigger Receiver Module is found in [12].

C. Busy Handling

1) Introduction: The busy handling is done by the BusyBox. The BusyBox is a dedicated board with two Xilinx Virtex-4 FPGAs and a DCS board on top.

The task of the BusyBox is to let the trigger system know when the detector is busy and can not handle new triggers. The sub-detector is considered busy when it is sampling data from a previous triggered event or when the buffers on the FEE are full. To perform its task the BusyBox needs to know what triggers are issued and how many buffers are occupied in the FEE. The trigger system will not send additional triggers as long as the busy signal is asserted.

The trigger information is acquired by the Trigger Receiver Module communicating with the local TTC system. Since the BusyBox has a DCS bus width of 16 bits (opposed to 32 as it is on the RCU), a BusyBox bus-wrapper is added to the Trigger Receiver Module. For information regarding the status of the buffers, communicating directly with the FEE would be inconvenient because it is located inside the detector in the radiation environment. The solution is to communicate with the D-RORCs which receive the event data fragments from the FEE buffers. The trigger is issued with a unique event ID. The event ID is part of the CDH which will be shipped with the event data to the D-RORCs during a readout. By comparing the event ID from the trigger with the event ID from the D-RORCs the number of used/free buffers on the FEE can be calculated indirectly.

2) Basic Functionality: When the BusyBox receives a L0 or L1 trigger, it will assert the busy signal and wait for an L2 trigger. If the L2 trigger is a reject or it does not arrive in time, the busy signal will be released. If the L2 trigger is an L2 accept then it is assumed that a buffer in the FEE has been occupied. The event ID from this trigger will be extracted and pushed into a local queue. This queue will contain the event IDs of the events that are assumed to be somewhere in the system. Either they are stored in FEE buffers or being transferred to the D-RORCs. In general, if the number of event IDs stored in this queue is greater or equal to the total number of available FEE buffers (4 or 8) the busy-signal is not released.

To clear an event ID out of the queue it needs to be verified that all D-RORCs have received the data for this event.

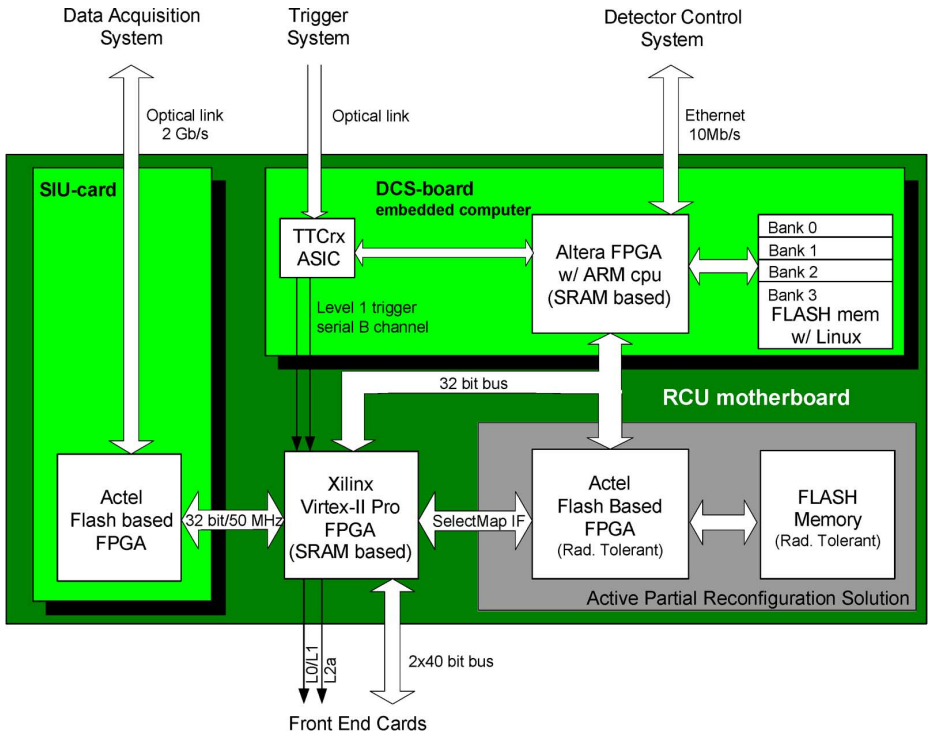

Fig. 7. Conceptual sketch of the RCU. The devices used for active partial configuration are highlighted bottom right.

The BusyBox requests the latest received event ID from the D-RORCs, and if, for some reason, a D-RORC doesn't reply, the BusyBox will resend the same request to the given D-RORC. This is important to not loose the synchronization of the events between the BusyBox and the individual D-RORCs.

The BusyBox will be used for several sub-detectors in ALICE such as TPC, PHOS, Forward Multiplicity Detector (FMD) and ElectroMagnetic CALorimeter (EMCAL).

IV. Radiation Tolerance

A. Introduction

The onboard FPGA on the DCS board cannot be used to receive the trigger data, as it is sensitive to SEUs. An SEU can lead to a Single Event Functional Interrupt (SEFI). Irradiation tests done of the Altera FPGA at the The Svedberg Laboratory in Uppsala, Sweden and at the Oslo Cyclotron Laboratory in Oslo, Norway has shown that for all 216 DCS boards used in the TPC detector, a number of 3–4 SEFIs can be expected per 4 hours run [9]. It is not a high number, but it is high enough to worry. If a SEFI occurs in the DCS board FPGA when it is used to access trigger information from the TTCrx registers, valid events might be lost. To prevent this, the Trigger Receiver Module is added to the RCU Xilinx FPGA firmware. In this way, all sensitive data are decoded and cached in the FPGA of the RCU board.

SEUs are not of a permanent nature and can be corrected by reloading the firmware into the configuration memory of the FPGA. The firmware files are stored in radiation tolerant flash memories on the different boards. On suspicion of an SEU in the DCS FPGA, a reboot will reload the configuration memory and the error will be gone. Since the data-path and the trigger-path is independent of the status of the DCS board FPGA, occasional downtime of the DCS board can be tolerated.

The RCU Xilinx FPGA is part of the data-path and a complete reconfiguration of this FPGA is not acceptable. Such an approach will interrupt the data-flow. To deal with this problem, two additional radiation tolerant devices are added on the RCU motherboard; an Actel ProASICPLUS APA075 flash based FPGA [13] and a Macronix MX29LV640 flash device [14] (see Fig. 7). The Actel FPGA communicates with the DCS board, the RCU flash device and the Xilinx SelectMAP interface. The SelectMAP interface is the fastest of the different configuration memory interfaces available on the selected Xilinx device. This facilitates Active Partial Reconfiguration of the Xilinx Virtex-II FPGA independently of the status of the DCS board.

Before selecting the Xilinx Virtex-II pro device other possibilities were discussed. With an ASIC the design time would have been significantly prolonged and it would be impossible to do firmware upgrades at a later stage. Flash based FPGAs did not offer the resources needed at the time when design was specified, and the radiation tolerant, SRAM-based FPGAs were too expensive. The commercial Xilinx FPGA was selected because of the configurability of such a device, the prize and the active partial reconfiguration which offered a way to deal with the radiation problems.

B. Active Partial Reconfiguration

Active Partial Reconfiguration is to overwrite the configuration memory of the FPGA without interrupting operation of the active design. This means that it is possible to clear an SEU immediately after it has occurred, hence minimizing the risk of a SEFI.

The Active Partial Reconfiguration solution on the RCU board has three main modes of operation: Initial (or full) configuration, full partial reconfiguration (or scrubbing) and frame by frame read back, verification and correction.

Initial configuration is done either on power-up or on command from the DCS board. The configuration file is stored on the RCU flash device. Scrubbing means overwriting the complete configuration memory, regardless of whether there has been an error or not. The file used for scrubbing is stored on the RCU flash device and the scrubbing is done on command from the DCS board, either once or continuously. The smallest accessible part of the configuration memory is called a minor frame (more often referred to as a frame). When doing frame by frame read back, verification and correction, the frames are read back from the Xilinx and verified with frames stored on the flash device. If a difference has been found it is immediately corrected by overwriting the given frame on the FPGA. This mode is executed either one frame at the time or continuously looping through all frames. The files used for initial configuration and scrubbing are generated by the Xilinx ISE software, while the frame files are generated by reading back the configuration memory in a controlled lab environment. There are certain restrictions on the utilization of resources in the FPGA when doing Active Partial Reconfiguration. This can lead to an increase of the used area of the design. More details on the Active Partial Reconfiguration solution can be found in [15].

Active Partial Reconfiguration will not prevent SEUs from occurring. If the SEU is in a critical element, such as a reset network or the clock routing network, the functionality of the Xilinx will most probably break down. Still, based on irradiation tests that have been performed by our group, Active Partial Reconfiguration is expected to reduce the influence of SEUs to a negligible level, especially if combined with conventional error detection and correction coding techniques. It is hard to generally quantify the effect of Active Partial Reconfiguration since it is highly design dependent. One of the main advantages of Active Partial Reconfiguration is that it reduces the risk that several SEUs combined causing permanent damage to the FPGA, for instance by changing the direction of an IO cell.

V. Summary and Conclusion

This article has discussed the Trigger System in the ALICE detector, with special focus given to the Front End Electronics of the TPC and the PHOS sub-detectors. The TPC detector has been through a commissioning period with extensive testing of all features including trigger handling for more than half a year. During this period the trigger reception for the TPC Front End Electronics has been tested with the previous version of the Trigger Receiver Module and by using a local Trigger, Timing and Control system that are running Central Trigger Processor emulator software. Real physical triggers have been used either coming from scintillators detecting cosmic radiation or by controlled laser beams.

One out of five PHOS modules will be installed during ALICE commissioning. The last four modules will be installed later with a second generation Trigger Router Unit that is relying on a Xilinx Virtex-5. This device has a more favorable architecture than the currently used Virtex-II pro device [7]. Trigger Router Unit firmware upgrades are expected to utilize the advantages of the Virtex-5.

The firmware for the Trigger-OR and the BusyBox is currently being designed, and the Trigger-OR will be commissioned with a lightweight version of the firmware. Future upgrades might also be interesting for the Front End Electronics trigger reception, for instance by adding more software and calibration trigger definitions if specified.

One of the main advantages with the Active Partial Reconfiguration solution is that, additionally to correcting SEUs, firmware upgrades can be easily done at any point via software for all presented sub-systems that includes a Xilinx device. This makes handling of triggers in the Front End Electronics configurable and easily adaptable for possible future demands.

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