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Power control and monitoring in the proton CT instrument

B023EB-14

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May, 2023

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Working on, and being a part of, the pCT project has been an exiting experience, and we want to thank the pCT team for involving us in the team meetings and making our work feel valuable.

Thank you to all the contributors at the microelectronics lab.

Abstract

The Proton CT project is a project that aims to create a CT machine where protons are utilized rather than photons. For use with proton cancer treatment, this has an advantage over traditional X-ray imaging with photons in the form of a more precise dose delivery through reduced uncertainty in photon to proton conversion. The project utilizes CERN-developed ALPIDE chips, originally developed for the ALICE project. By using these chips in multiple layers, a digital tracking calorimeter is formed, which can accurately create 3D images of the scanned object or person. The ALPIDE chips require a stable, reliable, low noise power source to operate.

This thesis seeks to improve the power delivery system for these chips. Included in this work is a redesign of a *Monitor Board*, whose function is to filter and monitor the current delivered to the ALPIDEs. Software for the Monitor Board is developed, along with a new communication protocol for communication between the Monitor Board and a *Monitor Board hub*, a Kintex Ultrascale FPGA KCU105 Evaluation Kit, that connects to a central control room. A draft for an *Adapter Board* for the hub is made, allowing for up to 43 Monitor Boards to connect to the KCU105. An expansion of the system is made in the form of a new custom *Backplane*, which distributes the current delivered from power supplies, through the Monitor Boards and on to the ALPIDEs.

Sammendrag

Proton CT prosjektet er et prosjekt som har som mål å designe et CT-apparat som benytter protoner til fotografering, heller enn fotoner. Til bruk sammen med strålebehandling med protoner har dette den fordelen over vanlig røntgen at doseplanleggingen blir mer presis gjennom at man slipper unna usikkerheten i omregningen fra fotoner til protoner. Prosjektet bruker CERN-utviklede ALPIDE chipper, opprinnelig utviklet for ALICE prosjektet. Ved å bruke disse chippene i mangfoldige lag, danner man et digitalt kalorimeter, som kan skape 3D bilder av det skannede objektet eller en person. ALPIDE chippene trenger en stabil, pålitelig, lavstøys strømforsyning for å operere.

Denne avhandlingen forsøker å forbedre strømforsyningssystemet til disse chippene. Inkludert i dette arbeidet er det et redesign av et *Monitor Kort*, som har som oppgave å filtrere og monitorere strømmen som blir levert til ALPIDE chippene. Software til Monitor Kortet blir utviklet, sammen med en ny kommunikasjonsprotokoll for kommunikasjon mellom Monitor Kortet og en *Monitor Kort hub*, en Kintex Ultrascale FPGA KCU105 Evaluation Kit, som er koblet til et kontrollrom. En skisse for et *Adapter Kort* for hub-en blir tegnet, som muligjør tilkobling for opp til 43 Monitor Kort inn på KCU105. En utvidelse av systemet blir laget i form av et spesiallaget *Bakplan*, som distribuerer strøm fra strømforsyninger, gjennom Monitor Kortene og ut til ALPIDE chippene.

Contents

Acronyms

AC Alternating Current

ADC Analog-to-Digital Converter

ALICE A Large Ion Collider Experiment

ALPIDE ALICE Pixel Detector

AVDD Analog voltage

CERN European Organization for Nuclear Research

CT Computed Tomography

DAC Digital-to-Analog Converter

DC Direct Current

DGND Digital Ground

DTC Digital Tracking Calorimeter

DVDD Digital voltage

FIFO First In First Out

FPGA Field Programmable Gate Array

GPIO General Purpose Input Output

HP Horizontal Pitch

I2C Inter-Integrated Circuit

IDE Integrated Development Environment

IFT Department of Physics and Technology

LSB Least Significant Bit

LVDS Low-Voltage Differential Signaling

MB Monitor Board

MCU Microcontroller Unit

NC Not Connected

PCB Printed Circuit Board

pCT Proton Computed Tomography

PSU Power Supply Unit

RX Receive

SOBP Spread Out Bragg Peak

SW Software

TC Transition Card

TX Transmit

UART Universal Asynchronous Receiver-Transmitter

UPDI Unified Program and Debug Interface

USART Universal Synchronous and Asynchronous Receiver-Transmitter

UVVM Universal VHDL Verification Methodology

UiB University of Bergen

VHDL Very High-Speed Integrated Circuit Hardware Description Language

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Section 1: Introduction

This section introduces the project and the previous work of which this thesis builds on, and describes the motivation for why the project exists in the first place.

Section 2: Objective of this thesis

This section covers the changes that UiB wants implemented from the design we inherited and sets up the goals for the project.

Section 3: Requirements and analysis

The needs and requirements for the project is outlined in this section, along with our analysis of how these requirements are to be met.

Section 4: Realization of the solution

Section four details the technical spesifications of our new designs. This includes realization of a new monitor board, software for the monitor board, modified FPGA design, a backplane, and a draft for an adapter board.

Section 5: Testing

The section about testing contains test plans and results for the designs outlined in Section four.

Section 6: Discussion

A brief discussion about the progression of the project is found in Section six.

Section 7: Conclusion

This section concludes the project and describes any weaknesses in our designs, aswell as recommendations for work that can be done, but were outside the scope of our project.

1 Introduction

1.1 Contracting entity

University of Bergen (UiB) is Norway's second oldest university and today is one of the highest-ranked universities in Norway and the Nordic region. The university was officially established in 1946, but through the Bergen Museum, it has roots dating back to 1825 [1]. Today, the University of Bergen is among the largest in the country, with 20,124 students in 2021, and is a collaborator with both European Organization for Nuclear Research (CERN) and the European Space Agency [2]. The University of Bergen is also the main actor in the Bergen Proton Computed Tomography (pCT) project, which this bachelor's thesis is based on.

1.2 Computed Tomography

Computed Tomography (CT) examination is medical cross-sectional photography that uses X-ray radiation to create a detailed image of the body's internal structures. CT scans are often used to diagnose and monitor a variety of conditions, including cancer, heart disease and other internal injuries.

The process of CT examinations begins with the patient having a plastic needle inserted which will inject contrast material into the blood if needed. During the examination itself, the patient lies on a motorized bench which moves the patient through the instrument so that it can take pictures from different angles.

The examination is then carried out by shooting a dose of X-ray radiation through the body from one side of the machine, while on the other side there are detectors that measure the radiation. Since the different tissues absorb different amounts of radiation, an image of the body can be constructed [3].

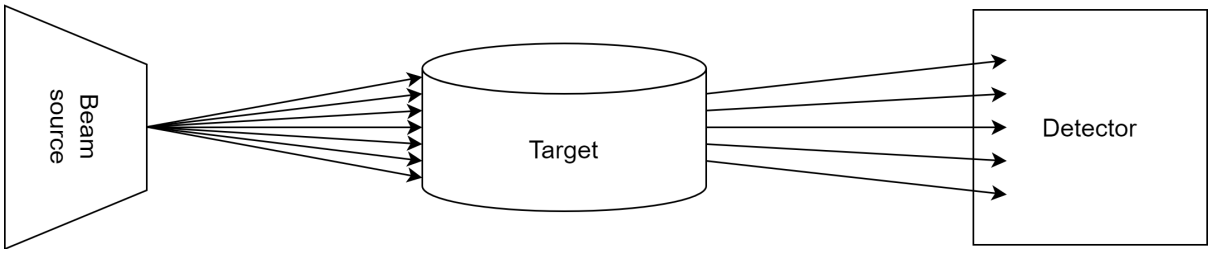

Figure 1.1: Simplified illustration of a CT examination. Illustration taken from: [4]

"Beam source" in Figure 1.1 refers to the X-ray beam that passes through the patient. The X-ray is photons [4].

1.2.1 Radiation Therapy

Today, two main methods are used to provide radiation therapy to patients, treatment with photon beams and treatment with proton beams. A third option, using heavier ions such as carbon, also exists, but is less widespread and is not the focus of this thesis. The common method is to treat with photon beams. Before treatment, a CT scan is done to

locate the tumor and calculate the radiation dose. This means that the patient is first examined using photon radiation and then treated using photon radiation.

The disadvantage of photon radiation is that much of the energy in the radiation is released a few centimeters after entering the patient. For example if a tumor is located 5 centimeters inside the tissue, much of the energy from the radiation will be deposited in healthy tissue surrounding the tumor. In contrast, this is the major advantage of proton radiation, which, characterized by its Bragg peak, release little energy besides at the top of the peak, as visualized in Figure 1.2. By aiming the Bragg peak to the depth of the tumor, proton radiation has the potential to cause less damage to healthy tissue during treatment. The red graph in Figure 1.2 represents the Spread Out Bragg Peak (SOBP) for protons. To achieve a SOBP, the energy from the beam is set so that the Bragg peak hits a certain depth, this is then repeated for the next depth and so on until the entire tumor area has been covered [5].

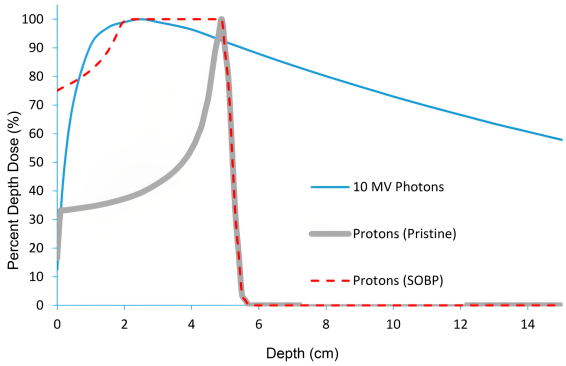

Figure 1.2: Bragg peak [6]

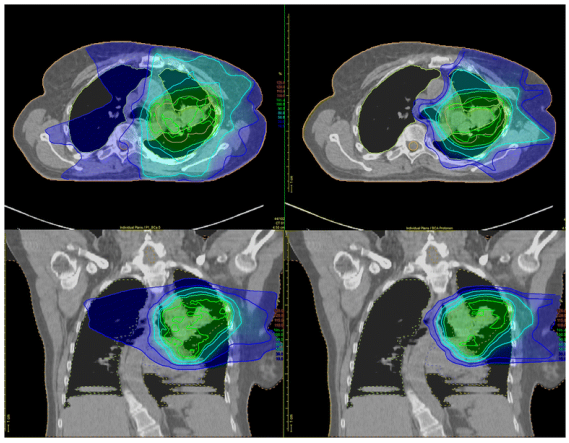

Figure 1.3: Photon vs proton [7]

Figure 1.3 shows the difference in dose delivery for photon radiation (on the left) and proton radiation (on the right).

1.3 Proton Computed Tomography

The motivation behind the pCT project is that today, when treating with proton radiation, X-rays (photons) are used through a conventional CT scan to map and plan the dose for protons. The conversion from photon imaging to proton radiation results in an unwanted uncertainty, and it can result in the treatment damaging more healthy tissue than necessary. The goal of the pCT project is to design an instrument that will offer patients more precise dose planning through proton radiation imaging. The instrument, called a Digital Tracking Calorimeter (DTC), measures the proton particle's exit angle and energy when the patient is exposed to protons. These data describe the relative stopping power of the protons and can be used to create more accurate dose plans than those obtained via X-rays [8].

The theory behind the pCT project is that during a pCT scan, the Bragg peak is set to hit the calorimeter. The calorimeter measures the angle and energy emitted, and by doing this from different angles, a 3D image of the patient and location of the tumor

can be formed. Then, the Bragg peak is calibrated to hit the tumor, and the patient is treated with a proton beam as described by the dose plan that has been calculated.

1.4 The Bergen proton CT project

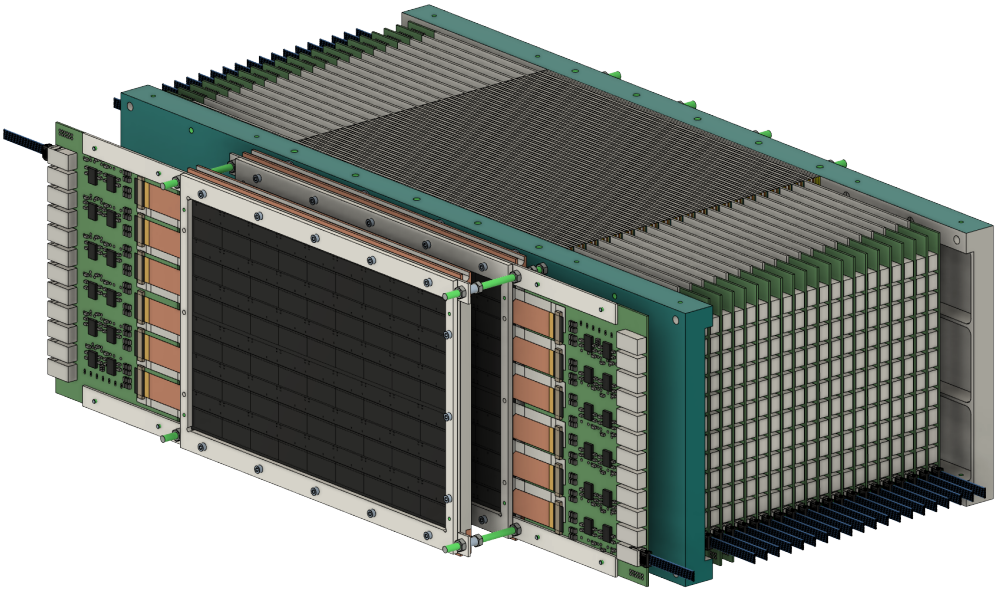

Figure 1.4: 3D design of the Digital Tracking Calorimeter

The calorimeter consists of 43 layers of ALICE Pixel Detector (ALPIDE) chips; two tracking layers and 41 calorimeter layers [9], where each layer contains 12 rows of chips, and each row contains 9 chips. A total of 108 chips per layer. The ALPIDE chips were developed for the ALICE experiment at CERN. Each chip records whether it has been hit by a proton, and by placing several layers behind each other, tracks can be created based on individual hits. Between each chip, there is an aluminum layer in place to slow down the particles, and by looking at where a track stops, the amount of energy the proton had when it hit the pCT detector can be determined.

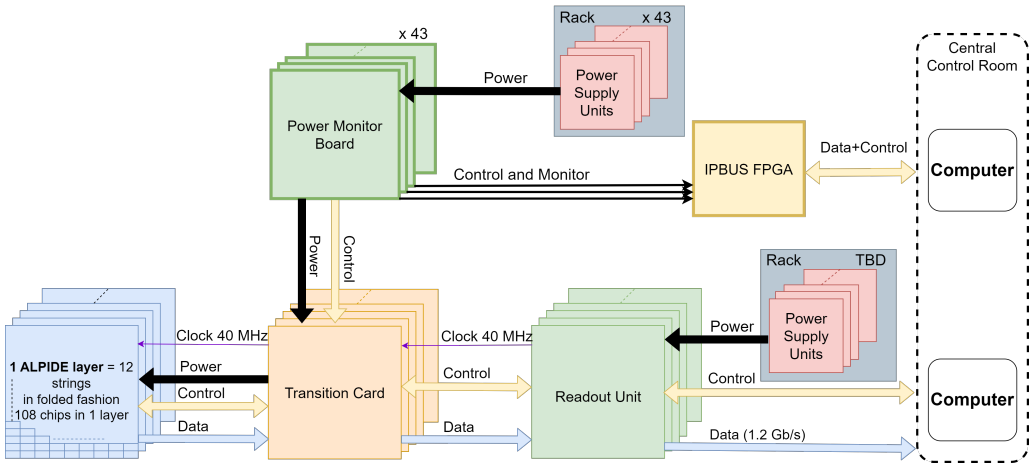

Figure 1.5: The current pCT ecosystem.

The calorimeter is part of an ecosystem built up by several bachelor, master, and PhD

theses written in connection with the pCT project. Figure 1.5 shows the current ecosystem, where the ALPIDE chips are connected to a Transition Card (TC) that supplements the chips with power from voltage regulators, and converts the connections from the chips from flexprint cable to firefly connectors. The TC card is then forwarded with logic for data reading, control and monitoring of the power supply to the TC card and the ALPIDE chips.

1.4.1 pCT Power

The part of the system which consists of control and monitoring of the power supply to the chips, which this bachelor's thesis will focus on, is marked with colors in Figure 1.6.

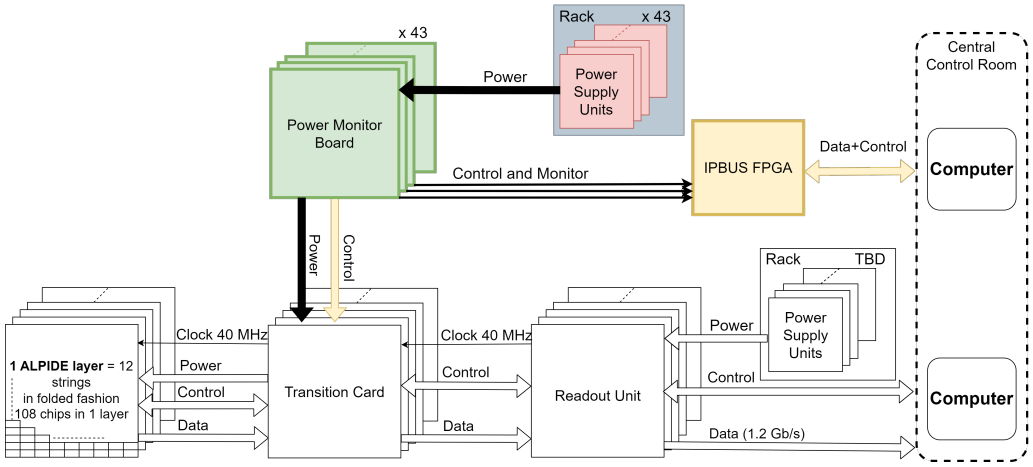

Figure 1.6: pCT power ecosystem

The existing system is designed to be supplied with power from MAX 105 series power supplies [10], with one Power Supply Unit (PSU) supplying one layer of 108 ALPIDE chips. The power supplied is to be monitored and filtered by a Monitor Board (MB), a custom-made card that houses a microcontroller which monitors the chips. Currently, the design calls for one monitor board to monitor one PSU. Therefore, the current design requires 43 PSUs and 43 monitor boards.

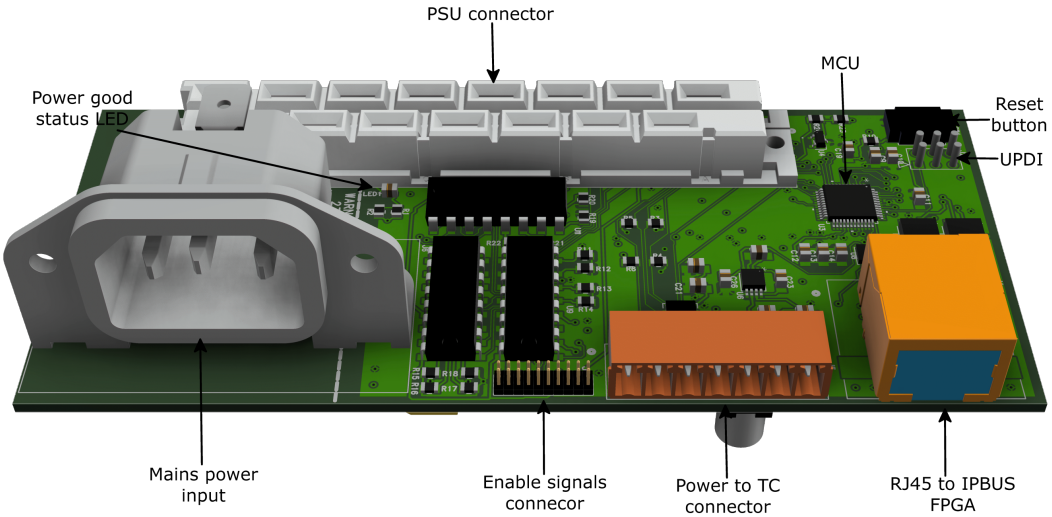

Figure 1.7: Previous monitor board design

In Birger Olsen's master's thesis [8], a solution is outlined where monitor boards are mounted in pairs with PSUs, which is then mounted with up to eight such pairs in a rack. This setup requires six racks to house the power supplies and corresponding MBs. Figure 1.8 shows Birger's envisioned stackup with the PSU and MB. Figure 1.9 shows the pairs mounted in a 3U rack.

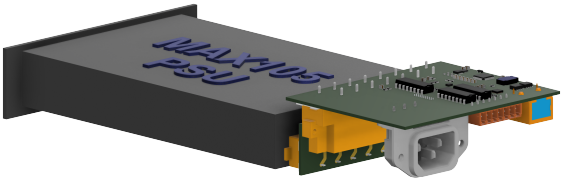

Figure 1.8: PSU and monitor board

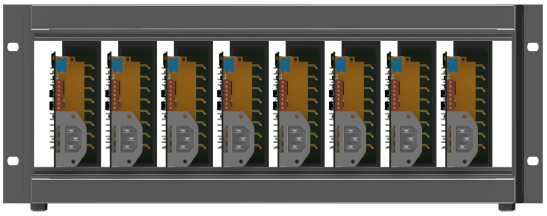

Figure 1.9: Rack

The main objective of these power supplies is to be mountable in standard subracks that fit into standard racks. This provides flexibility in terms of mounting, procurement and maintenance.

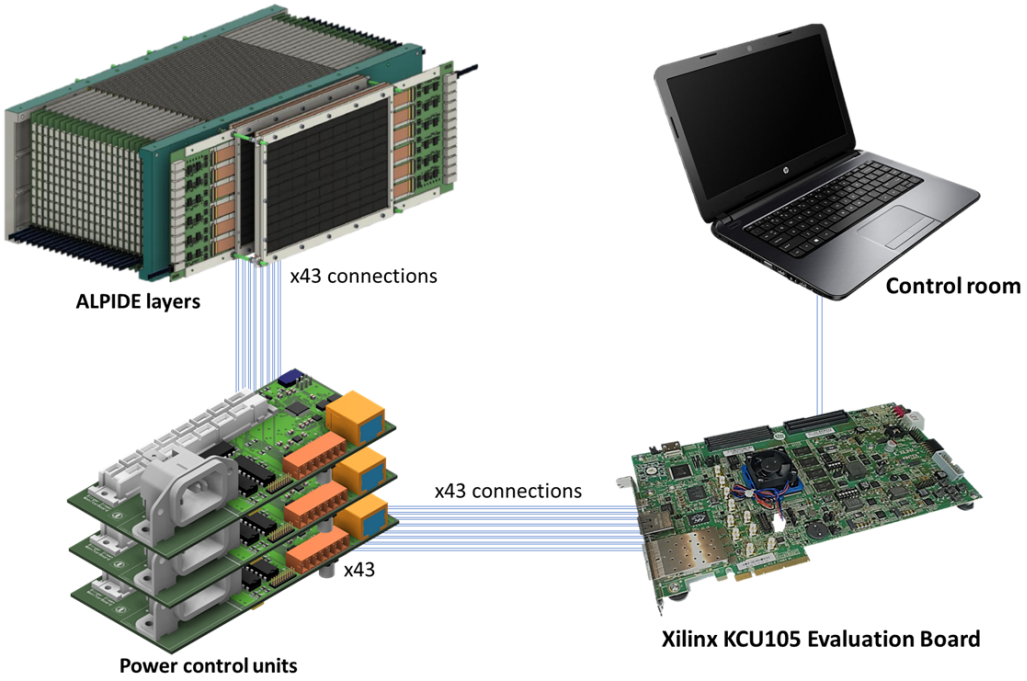

Figure 1.10: Simplified overview of pCT power. Overview provided by Jacob Hauser and Martin Eggen [11]

A simplified version of the power monitoring system is shown in Figure 1.10. With the help of a Xilinx FPGA, communication with the microcontrollers on all 43 monitor boards can be established through RJ45 connectors. The FPGA, which we from now on will call the "Monitor Board HUB", or simply "MB HUB", monitors all of the monitor boards. All information about different values and thresholds is available for reading and writing to by the user. The MB HUB, which was developed by Eggen and Hauser in an earlier bachelor's thesis [11], communicates with the control room using the IPbus library [12].

2 Objective of this thesis

The inherited design shown in the introduction, with monitor boards mounted directly to the power supplies, forms a strong base for the power delivery solution. It also presents a few issues to be solved:

- AC power is passed through the monitor board to the power supply, instead of directly to the power supply.
- By having the power connector on the monitor board, a total of 43 power cables are needed, one for each monitor board and PSU.
- Since the monitor board is only mounted to the PSU via a DIN connector, it is susceptible to damage from movement, either from plugging it into the PSU or from plugging cables into the board itself.
- The communication protocol between the microcontroller and the FPGA has a clock skew bug

The objective of this thesis is to build on and expand the inherited design, while addressing these issues.

Based on this, UiB set out the following goals:

Prioritized:

- Draw a new rack design with a backplane PCB which acts as a connection between the monitor boards and the PSUs, see Figure 4.49.
- Design the new backplane card to fit into the rack, see Figure 4.19.
- Design a new monitor board based on the old design, that can plug into the backplane in the rack, see Figure 4.1.
- Fix the clock skew bug in the microcontroller software, and ensure steady communication between the microcontroller and the MB hub. This also involves modifying the MB hub FPGA design to accomodate a new communication protocol.

Optional:

- Sketch an adapter board design for connecting all the RJ45 connectors from the monitor boards into the MB hub.

3 Requirements and analysis

3.1 Specification of requirements

The requirements for the power delivery system, as one entity, is given by the following:

1. "Supply stable power of at least 3.3 V to the TC, low noise (<1 mV). The power supply solution should be no closer than 5 m to the DTC [8, p. 5]."
2. "Be able to deliver at least 13.2 A of current. 2.4 A to AVDD and 10.8 A to DVDD [8, p. 5]."
3. Distribute 230 VAC to multiple power supplies without having to use external cables.
4. Filter the current delivered to the ALPIDE chips, particularly from noise made by the power supplies.
5. Monitor the current delivered to the ALPIDE chips, and shut off the supply in case of the current draw exceeding the set limits.
6. Communicate with a central control room via IPbus.

To facilitate a more robust system, each single TC should have its own dedicated PSU and MB. That will prevent cascading failures if one part fails.

3.2 Analysis

The possibilities for designing a system which covers the these requirements are endless, but if we are to follow the goals outlined in Section 2, we can make the following updated drawing of the ecosystem:

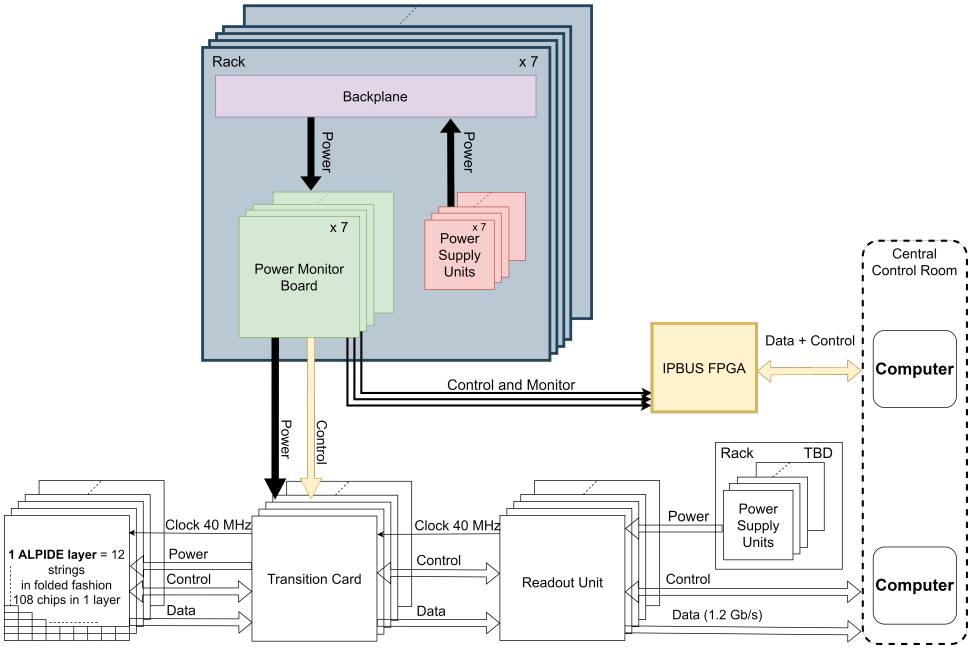

Figure 3.1: Updated pCT ecosystem

This rest of this section will split the system into three separate subsystems, and discuss the distinct requirements for each of the subsystems;

1. The monitor board hardware

2. The software for the monitor board, along with the VHDL for communication with the monitor board hub.

3. The backplane.

3.2.1 Monitor Board hardware

1. Needs at least one Universal Asynchronous Receiver-Transmitter (UART) interface to communicate with the MB hub.

2. Must be capable of transfering at least 13.2 A worth of current as per Birger Olsen's earlier calculations [8].

3. Has to fit within the standard "EuroCard" format (160 mm x 100 mm).

4. Needs a 7-pin Weidmüller connector to support the powerlines for 2xDVDD, 2xAVDD, their respective grounds, and PWELL.

5. The PWELL signal should be possible to regulate between 0 V and -6 V.

6. Needs circuitry to handle a PT1000 temperature sensor.

PWELL is the bias signal for the ALPIDE chips. It works by changing the voltage at the p-type wells in the silicon. This change in voltage allows the user to change the sensitivity of the silicon chips.

3.2.2 Software and VHDL

1. Should retrieve sensor data without blocking the UART interface.

2. Measure the current draw of each string of ALPIDE chips.

3. Implement a soft startup to avoid a large inrush current.

4. Each of the 12 enable signals should be able to be toggled individually.

5. Temperature should be measured and logged.

6. Implement a register based interface for the MB hub.

3.2.3 Backplane

The backplane has five main tasks, as it needs to:

1. Supply the PSUs with 230 V Alternating Current (AC) voltage.
2. Connect the PSUs together with the MBs in pairs, without having to use cables or power rails.
3. Be able to deliver a 16 A current over 5 V continuously from the PSU to the MB, in each pair.
4. Secure a path to ground from the MB.
5. Fit into a 19 inch subrack, interconnected with the MBs and PSUs.
6. Have a thickness of $\geq$ 2 mm, to be rigid and handle connectors being plugged in and out reasonably often.

3.2.4 Version control

This project also requires a version control system to be used. The version control system of choice is Git, and the repository is hosted on UiB's GitLab server.

3.3 Regarding development tools

This section discusses the tools used for developing a Printed Circuit Board (PCB), aswell as the firmware for the Microcontroller Unit (MCU) on the MB and the Hardware Description Language for the Field Programmable Gate Array (FPGA) design.

3.3.1 PCB development

While the list of available tools for developing a PCB is long, our choice ultimately ends between the software our group has experience with from before, and the software that the Department of Physics and Technology (IFT) at UiB uses.

Table 3.1 looks at the advantages and disadvantages of the two of them:

	Advantages	**Drawbacks**
KiCAD	Open source Prior experience in the team Lower threshold for new users	Less built in tools and options Less restrictive - more room for errors
Xpedition	Used by IFT More tools at disposal Safety mechanisms restricting user errors	No prior experience Large barrier of entry - difficult for inexperienced designers

Table 3.1: KiCAD vs. Xpedition

The advantage of using the same schematic- and PCB layout tool as the department weighed heavily in favour of using Xpedition, which ended up as our program of choice. This meant that the inherited design files could immediately be implemented in the process of designing the new boards, while also making it easier for the department to make changes to the designs after our bachelor's report is finished.

3.3.2 Software development

In terms of writing the firmware for the MCU on the MB, the two closest available alternatives were to either:

1. Use the chip-manufacturers proprietary Integrated Development Environment (IDE) for the AVR chip

2. Use Visual studio Code with "PlatformIO"-toolbox

Both IDEs are able to debug the firmware before programming, so this choice is merely one of taste. Due to having used Visual studio Code extensively from before, it has been our choice for this project.

To aid with testing of the firmware before the redesigned MB is finished, AVR128DA48 development boards are used as placeholders.

3.3.3 VHDL development

Since the FPGA used in this project is a Xilinx KCU105 evaluation board, we used Xilinx Vivado as our development tool. The required license for this tool is provided by IFT.

When writing Very High-Speed Integrated Circuit Hardware Description Language (VHDL), it is important to be able to verify that the code is working as intended. This is done by simulating the code. Since we had previous experience with ModelSim and this was the simulator used by IFT, we chose to use this simulator.

4 Realization of the design

4.1 Monitor Board

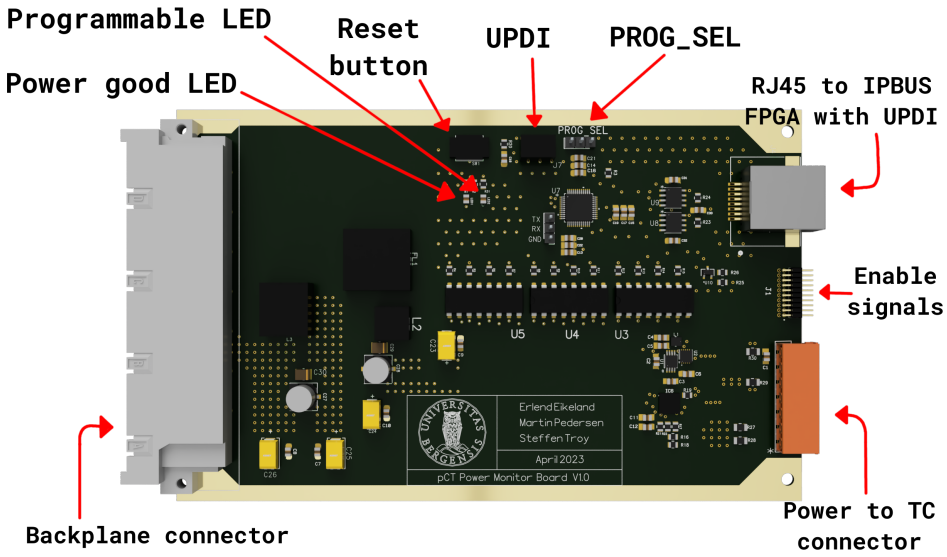

Figure 4.1: Monitor board overview

The figure above shows a render of the realized design for the MB. The functionalities of the MB are simplified in the render.

4.1.1 Block diagram

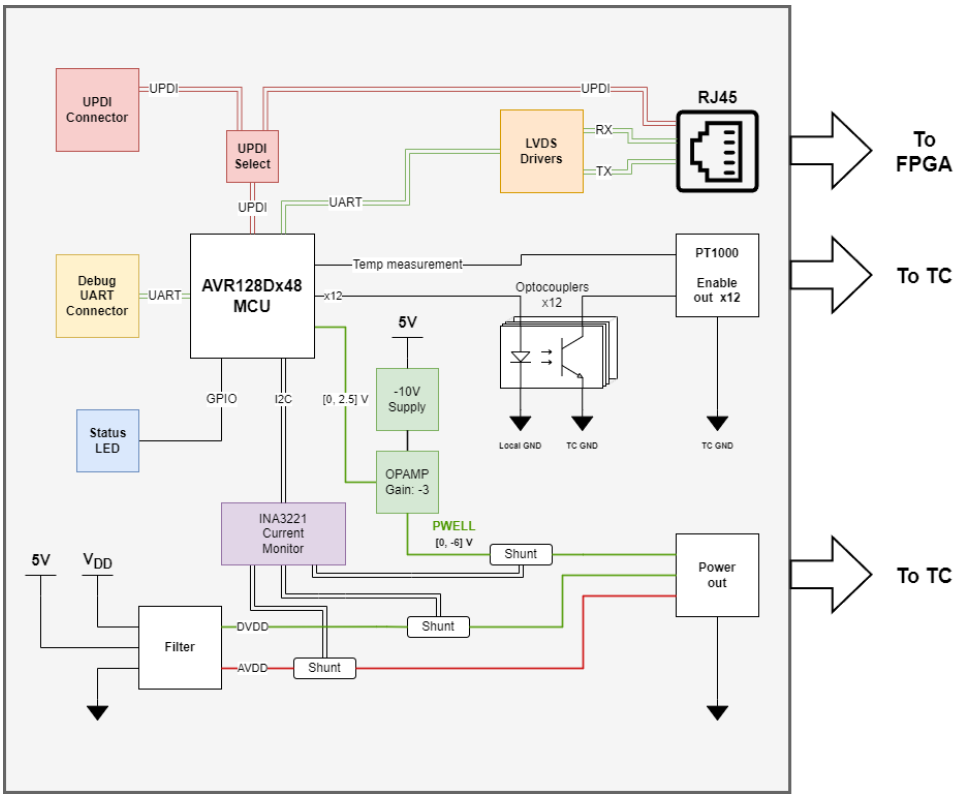

Figure 4.2: Block diagram of the Monitor Board

Figure 4.2 shows the entire device as a simplified block diagram. The DIN41612 connector has been ommitted for simplicity. The center piece of the device is the microcontroller which is labelled as AVR128Dx48, which reference the fact that it can accept both the DA and DB families of the AVR MCU lineup, and specifically the 128 kB Flash version, with 48 pins.

The PWELL circuitry shown in the block diagram above, creates a programmable voltage between 0 V and −6 V for adjusting the ALPIDE bias.

4.1.2 Power filtering

Since Birger Olsen has already designed and tested a filter circuit for the MB, we have chosen to use his design, as it is already proven to work. The design is a a filter using a common mode choke and a capacitor to ground. The MB features two of these filters, one for the digital voltage and one for the analog voltage. For a more specific filter design for both the DVDD and AVDD voltages, see C.2 and C.3 in the appendix.

The filter he designed was not suited for the current requirements of the pCT project, and the inductors had to be scaled up in both size and current rating to handle the full 13.2 A of current required by the ALPIDE chips. That current rating is divided unevenly between the two filters, where the Digital voltage (DVDD) filter has to handle $10.56A$ and the Analog voltage (AVDD) filter has to handle 2.64 A. This is explained in more detail in Section 4.1.3.

This did lead to some issues in the selection of new components for the filter. As the inductors were too small for the current requirements in Birger Olsen's design, they had to be scaled up. That meant finding similarly rated inductances with a higher current rating, which in turn means larger inductors in terms of volume.

For the common mode chokes in particular, a new issue arose where there were no parts available in the desired current range, leading to a massive increase in size, far beyond what was originally thought of. This was undesirable, however as there were no alternative "off-the-shelf" (as in readily available from manufacturers) components available, larger components were needed. While a few amps extra would have been welcome, that was not the case, and the new common mode choke for the DVDD filter is rated for 30 A, which is double the targeted 15 A rating. This massive increase in size, means that the choke no longer fits on the MB and has to be moved to the backplane instead, see Section 4.2.9.

4.1.3 Power supply

As Birger Olsen already had spent a significant amount of time on the power ripple filters, there was no desire nor demand to replace the existing power supply. The power supply is a MAX 105 series power supply from nVent Schroff[10], which is a 3U power supply that can deliver up to 80W of power at 5V and 16A. The power supply is shown in Figure 4.3.

Each TC consists of 12 ALPIDE strings, with each string consisting of 9 ALPIDEs [8]. Each string requires approximately 880 mA of current for digital operations, and 220 mA

for analog operations. In total, each TC requires 13.2 A of current. This means that the power supplies can only power 1 TC each.

Figuring out how much power the MB uses is not as straight forward as it has never been tested properly in the real world. Thus we have to calculate an estimate using the worst case scenarios given by the datasheets for the different components on the PCB.

1. MCU - 4 mA [13][14]

2. Optocouplers - 228 mA (19 mA each) [8]

3. PWELL - 21 mA [15]

4. LVDS - 60 mA (30 mA each) [16]

Adding these together gives us a theorethical total of 313 mA of current for the MB. However, it is worth noting that the Low-Voltage Differential Signaling (LVDS) drivers are capable of delivering up to 350 mA per channel [16], which together can mean a short circuit current of 700 mA. While this is still within the capabilities of the PSU, we do not consider it as part of the normal operating conditions as we do not expect the lines to be shorted during normal operations.

Adding the currents for the ALPIDEs and the MB together, gives us a theoretical max consumption of 13.52 A. This is well within the capabilities of the PSU as it can provide up to 16 A of current with a small headroom for potential current spikes. We cannot know for certain, though, until we have actually measured the current draw of the MB.

Figure 4.3: MAX105 series power supply

4.1.4 Communication

Originally Birger's design had an Universal Synchronous and Asynchronous Receiver-Transmitter (USART) interface for communication with the MB hub. However, there were a few serious issues that impacted reliability. Most notably, the USART had issues with clock skew and synchronization issues. This led to the decision to replace the synchronous USART interface with an UART as it is asynchronous.

This meant the physical interface had to also be changed. The old design utilized two LVDS circuits, one for clock and one for bidirectional data. As clock was no longer a necessity, we repurposed the clock channel to be a second data channel. Thus we could avoid bidirectional data over a single LVDS pair. This means we are now using one LVDS pair per direction, which gives us a total of two pairs just like the original design.

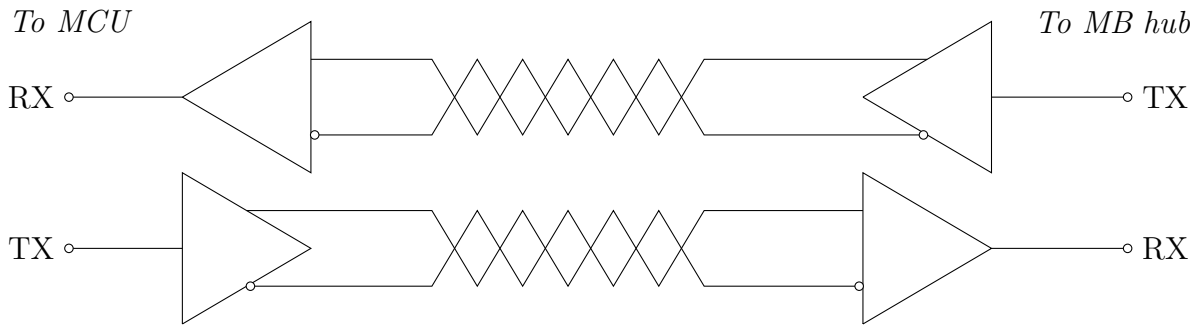

Figure 4.4: LVDS Circuitry

The LVDS works by transmitting the data as two opposite signals, one of which is inverted from the other. This means hat the receiver can subtract the signals from each other and get back the original signal. This is done to reduce the effect of noise on the signal. This is done as the noise will affect both signals equally, and when subtracted from each other, the noise will be mostly removed. The LVDS circuitry is shown in Figure 4.4. Another advantage is the lack of a common ground, which means that the LVDS can be used to transmit data between two devices that are not at the same ground potential. This is useful in our case as the MCU and MB hub are powered by different power supplies.

The LVDS wires are then connected directly to the modular connector on the front panel. This also means that there is no protection built in except what is already present on the RS-485 IC which is doing the conversion. Hence, the LVDS circuitry is very simple, and only consists of a few resistors and a termination resistor.

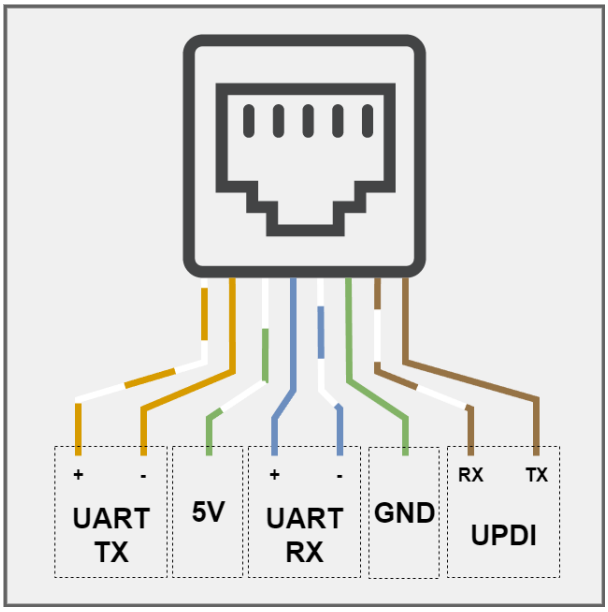

Figure 4.5: RJ-45 Connector Pinout

One thing to note in the figure above, is the fact that we are using all the pins available in the modular connector, this is for remote programming capabilities in the future.

4.1.5 Programming

The MCU is programmed via Unified Program and Debug Interface (UPDI) which is available on both the UPDI header, and the RJ-45 connector. Either can be used by simply moving the jumper on the *PROG_SEL* header. The UPDI connector is shown in Figure 4.6.

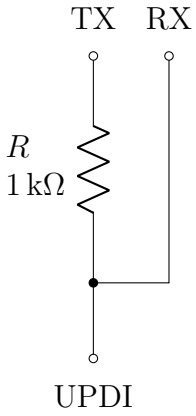

Figure 4.6: Programming circuitry [17]

UPDI Header

UPDI	1	2	VCC
NC	3	4	NC
NC	5	6	GND

Figure 4.7: Programming header

If the MB is already installed in a subrack, it may not be possible nor convinient to uninstall the MB each time one wants to reprogram it. Therefore we also have broken out the exact same UPDI pins to the modular connector on the front panel using the spare pins from the communication interface 4.1.4. The full pinout for this connector is shown in Figure 4.5.

4.1.6 Current monitoring

The current monitoring design has not been altered from the original design. It still features the INA3221 current monitoring chip.

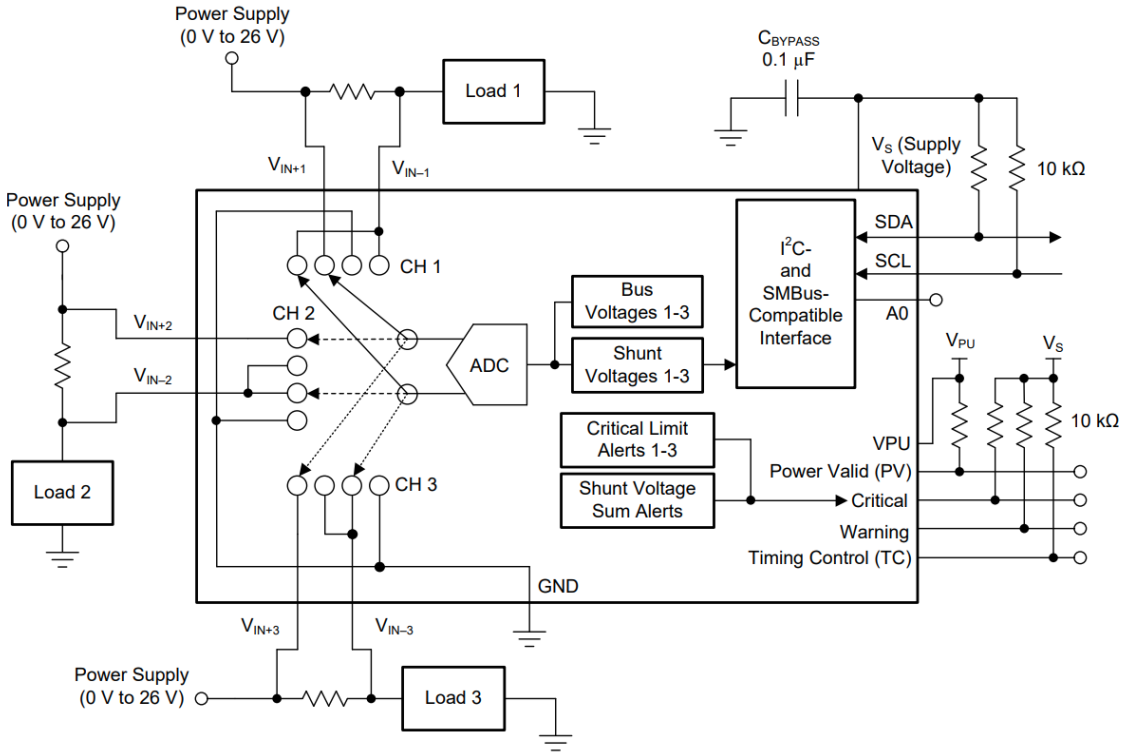

Figure 4.8: Diagram of the INA3221 current monitoring chip

This chip is capable of monitoring three separate channels, and combined with the 25 mΩ shunt resistors, it is capable of measuring currents with a resolution of approximately 160 µA on the PWELL and AVDD rails. The DVDD rail has two of these shunts in parallel giving them an effective resistance of 12.5 mΩ, which would give a resolution of approximately 320 µA. These values were calculated by dividing the shunt Analog-to-Digital Converter (ADC)'s Least Significant Bit (LSB) resolution of 40 µV [18] by the shunt resistance.

However, while it is nice to have a high resolution, this is hardly necessary for this application. The main advantage of such low resistances in this case, is their lower power dissipation. This allows us to use smaller resistors, which in turn allows us to fit more components on the PCB if required in the future.

4.1.7 Digital isolation

In order to avoid having the microcontroller influence the voltage quality of the TC power rails, the MCU is isolated from the TC power rails using optocouplers. Each Enable signal is connected to their own optocoupler, which is then connected to the MCU through a General Purpose Input Output (GPIO) pin. This allows the MCU to enable and disable the TC power rails without introducing any noise into the TC power rails.

This design has been kept from the original design Birger Olson did in his thesis [8].

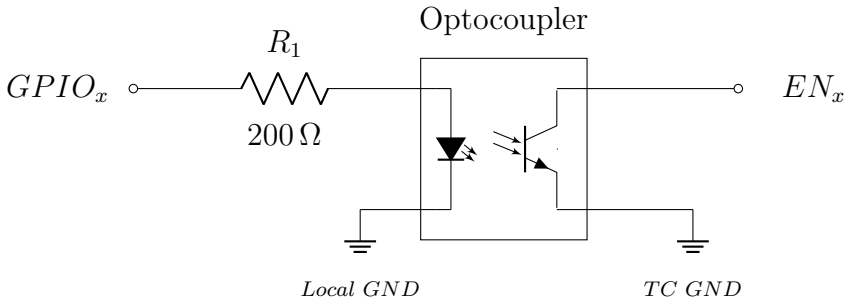

Figure 4.9: Optocoupler

4.1.8 Microcontroller

The heart of the MB is the AVR128Dx48 MCU. This is a 8-bit MCU family from Microchip Technology Inc. which features the robust AVR architecture. This microcontroller family was chosen mostly due to them being present on Birger Olsen's design, and thus there are already some work done on the software, and most importantly the hardware side of things. This means we can reuse a lof of the design, with the added advantage of having the chips in stock locally at the university.

However, the stock situation was not good enough to permit the same chip on all boards, thats why we have attempted to design it around the possibility of using both the DB and DA family of those chips, where the DB family is the one that was used in the original design. The reasoning for chosing DA as an alterantive chip was because it was mostly pin compatible with the DB family, while also being readily available as development boards for a reasonable price. This means that we can harvest the DA chips from these boards and use them in our design. The only significant difference between the two families is that the DB family features peripherals tailored more towards analog applications, which is not needed in this application.[13] [14]

4.1.9 Layout

The MB is designed to be a 6 layer PCB. This was to allow flexibility in routing and permit the higher current the PCB has to handle.

The PCB has been routed so that two layers are sacrifised to act as shielding between the analog sections and the digital sections. This reduces the noise that the digital sections might introduce to the analog sections.

4.1.10 Stackup

The specific PCB stackup of the MB is not considered important to meet its requirements. Therefore it does not feature any impedance matching or any special considerations beyond what was deemed the most practical in terms of layout and routing. The stackup is as follows:

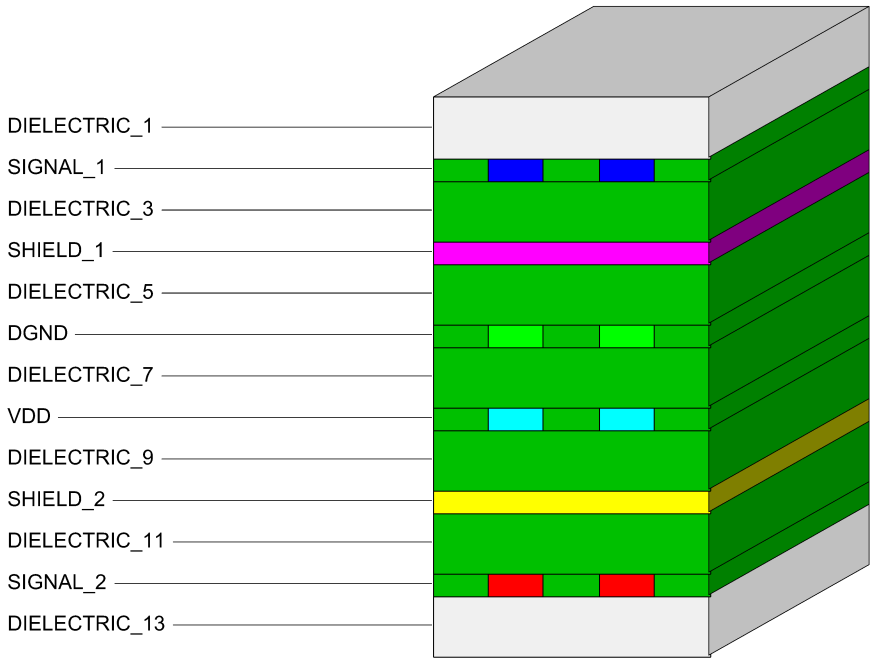

Figure 4.10: Monitor Board stackup

It is worth mentioning that both Top and the Bottom layer also features Signal and Chassis ground planes. These are not considered as layers in the stackup as they are not dedicated layers, but rather a part of the top and bottom layer. The lack of any special requirements also means the details on how thick each layer is, is not considered and has been chosen by which alternative was the most cost effective. However, it is important to note that the copper thickness has to be at least 35 µm to meet the the PCB's current requirements.

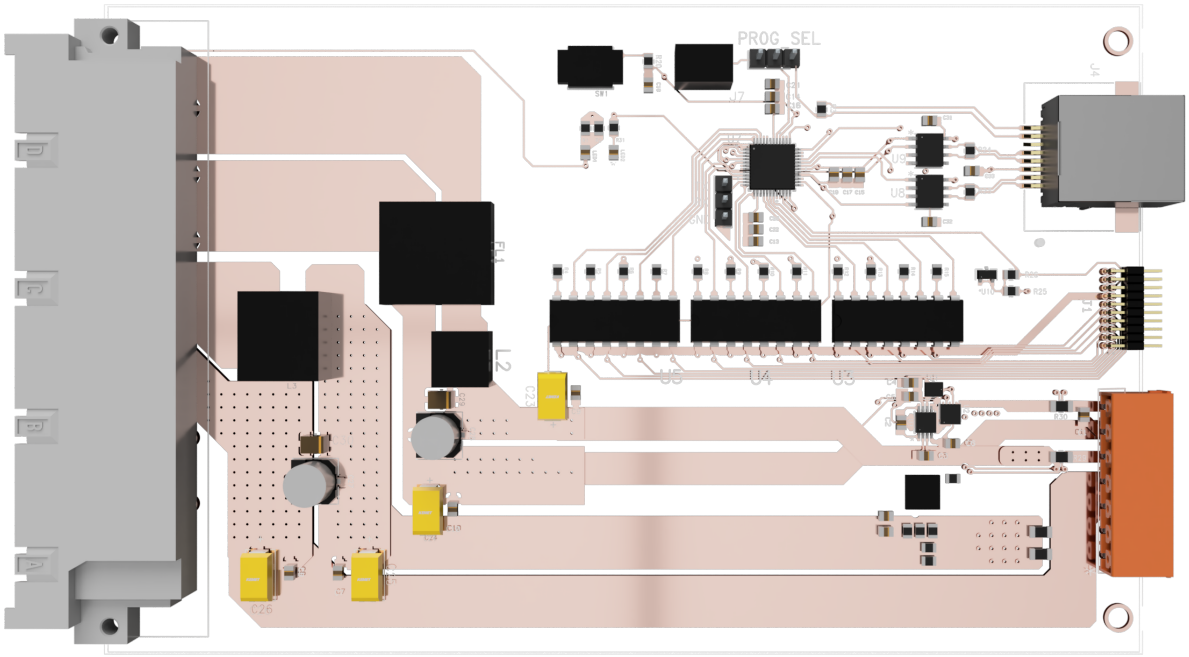

Figure 4.11: Monitor Board w/ reduced copper

Above is an image of the MB with the FR4 (the glass fiber substrate of a PCB), shield planes and parts of the silkscreen hidden to visualize the power connections better.

Figure 4.12: Closeup of the DVDD copper pour

The image in 4.12 shows the DVDD lines at the thinnest section. The copper pours have been placed next to each other in the figure in order to make them more visibl. They are placed in order of the stackup, where the pour closest to the top is the top most layer and the pour closest to the bottom is the bottom most layer.

Noticably at the bottom layer, there is a significant cut in the copper pour at the bend, this is to allow the placement of an exposed copper rail that allows for the board to be

grounded by its edges. Despite this, the width at the thinnest section is 3.536 mm at a thickness of 35 µm. With the other two layers which are both at a width of 7 mm at their thinnest, we should be well within the required current handling capabilities.

Using a tool like the Saturn PCB toolkit [19], we can quickly check their current capabilities at a modest 20 °C temperature rise above ambient. This PCB toolkit bases its calculations on the newest, relevant standard IPC-2152, for determining current carrying capacity in PCB-design [20]. The results of this can be seen in the figures below.

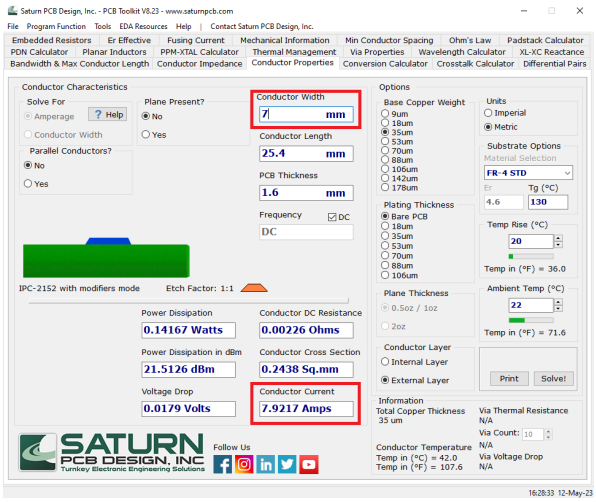

Figure 4.13: Saturn PCB toolkit calculation of a 7 mm wide trace

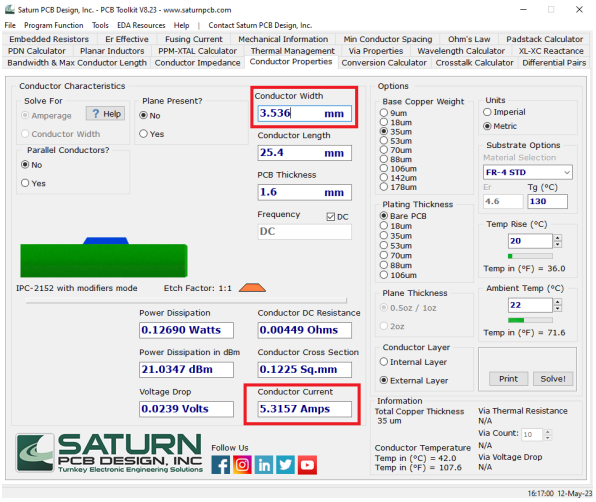

Figure 4.14: Saturn PCB toolkit calculation of a 3.536 mm wide trace

Since each copper pour act as a wire, we should be able to simply add the current capabilities together, which gives us a theoretical rating of 21.16 A. With 12 strings of ALPIDE chips on each MB, and using the current requirements as mentioned in 4.1.3, We should only expect a maximum current draw of 10.56 A, which means our design should be well withing the requirements.

As for the AVDD, not much thought has been given to that copper pour as its current requirements are significantly lower than the DVDD. At a measly 2.64 A at most, which was calculated by subtracting the maximum sum mentioned in 4.1.3 from the numbers given for the DVDD traces, as thin traces as 1.055 mm can handle the currents, but as we had the space, the copper pour was set to be 2.6 mm wide at its thinnest. While it is advantageous to have thicker traces for both current handling and heat dissipation, it does also present routing difficulties for other layers.

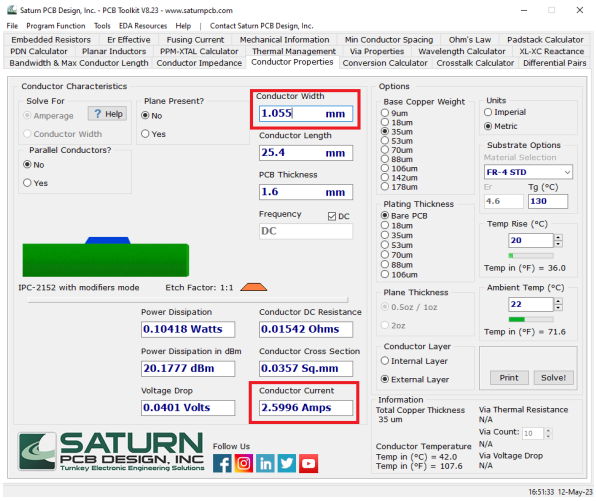

Figure 4.15: Saturn PCB toolkit calculation of a 1.055 mm wide trace

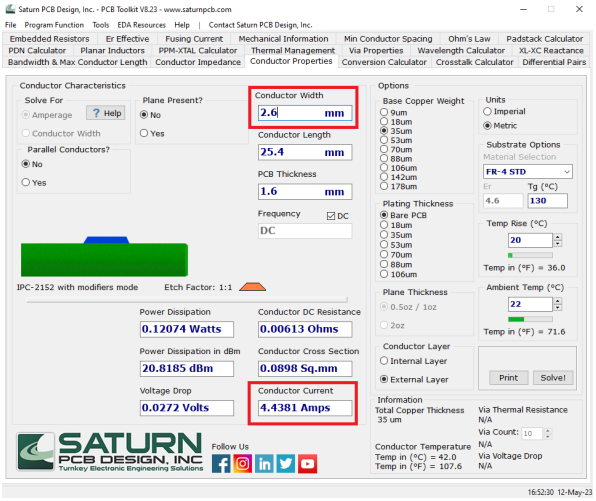

Figure 4.16: Saturn PCB toolkit calculation of a 2.6 mm wide trace

As a final note, most of the copper pours for both these current handling traces are thicker on most of their length, and does contribute positively to the current handling capabilities of the PCB through heat dissipation, which should allow even higher currents than the numbers above show. But as the current handling capabilities are already well within the requirements, this is not something that needs to be taken into consideration.

4.1.11 Revised Revised Form factor

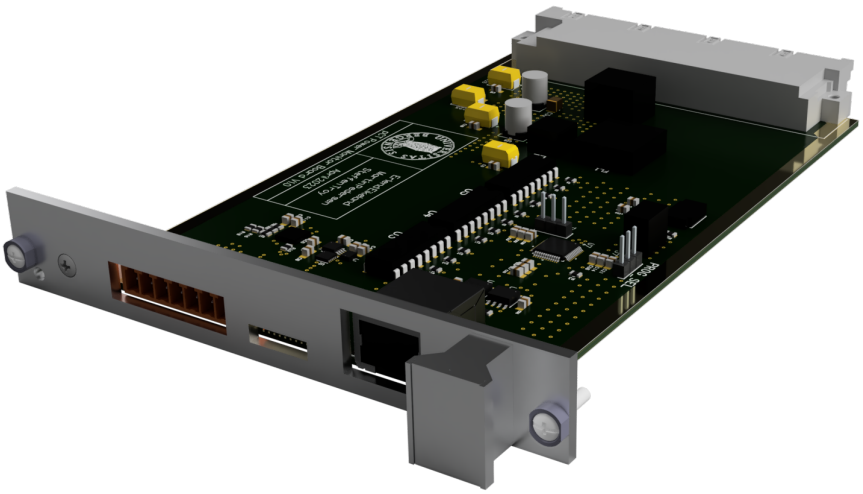

Figure 4.17: Monitor Board with front panel

The previous design featured a more compact design where each MB would sit on the connector of the PSU. That was later deemed structurally unsound and would require more cables than the updated design. The updated design features a more modular solution where each MB is paired with their own PSU through a common backplane. While it is configured to a 1:1 relation, that can be changed through a backplane redesign.

The MB themselves have been completely redesigned to fit in the "Eurocard" form factor. This is an industrial standard that is common in the industry especially here in Europe.

The design is to place the MB into a 19 inch subrack with height 3 U (units), and a width of 84 Horizontal Pitch (HP), which equals 84·5.08 mm = 426.72 mm, and 128.55±0.15 mm in height. These measurements are edge to edge measurements.

These subracks are available in heights of 3U, 6U and 9U, where this project has chosen the 3U variant due to the PSU already being designed to fit this form factor. 1U or 1 unit is equal to 44.45 mm in height, where our solution will take up 3 of these units or 133.35 mm in height. This gives us a PCB height of 100 mm and a card width of either 100, 160 or 220 mm, where we chose the popular 160 mm width. This was chosen as it would give us a decently large area to work on without being too big. This proved to be essential to make room for the issue that arose in the power filtering Section 4.1.2.

4.1.12 Design revisions

After the first prototype was produced and tested, a fatal flaw was discovered. The via connections to the microcontroller power lines are not present on the first prototype. This has been corrected in the current design files. There is however a need to correct the first revision of the PCB to make it functional. This is done by soldering thin magnet wire, or any other type of wire, from the areas affected to the nearest pad which is connected to VCC. This is shown in Figure 4.18 below.

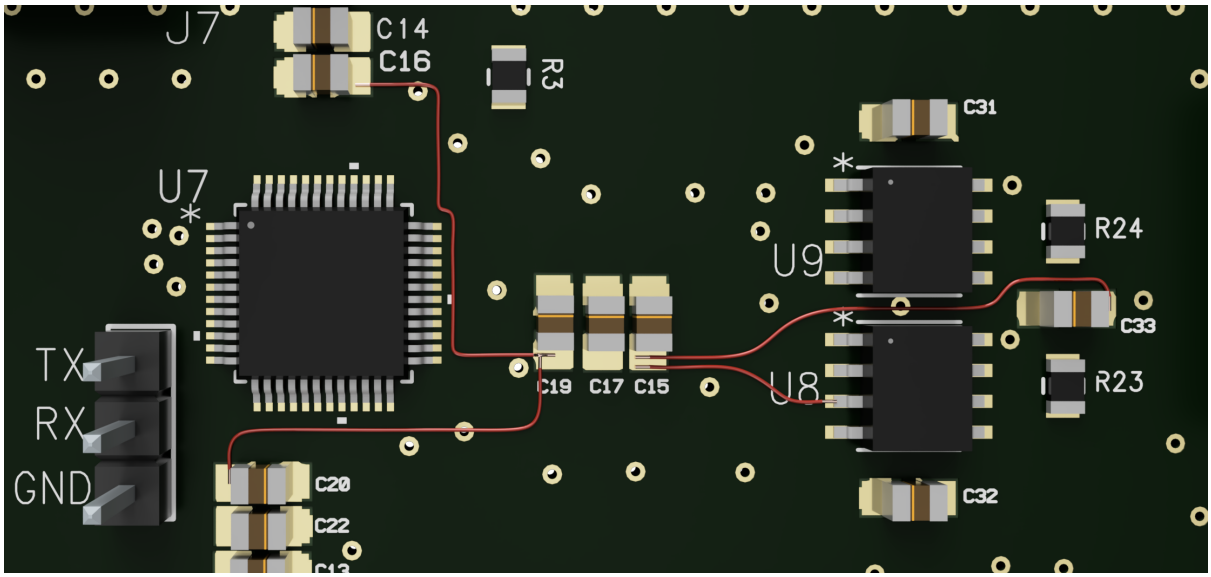

Figure 4.18: Monitor Board with fix

As shown, it is recommended to solder a wire between C19 and C20, between C16 and C19, between U8 pin 3 and C15 and between C15 and C33. This should restore power to the affected areas. The wires should be secured with kapton tape or similar to avoid melting during soldering.

4.2 Backplane

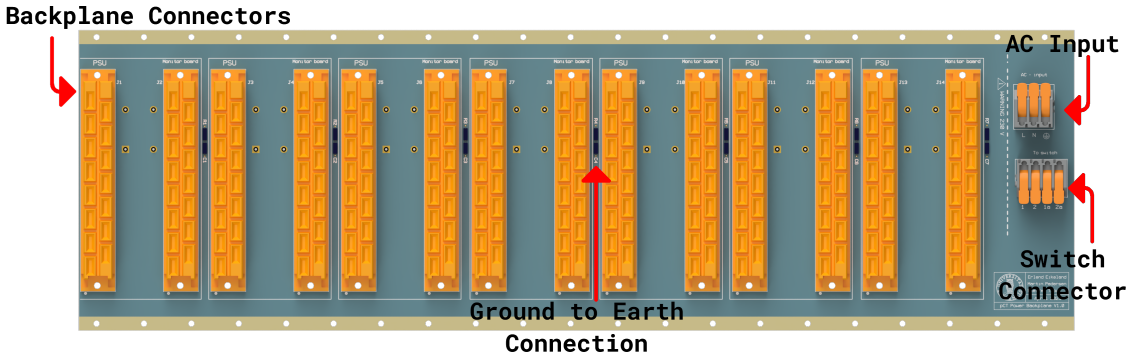

Figure 4.19: Backplane overview

4.2.1 Block diagram

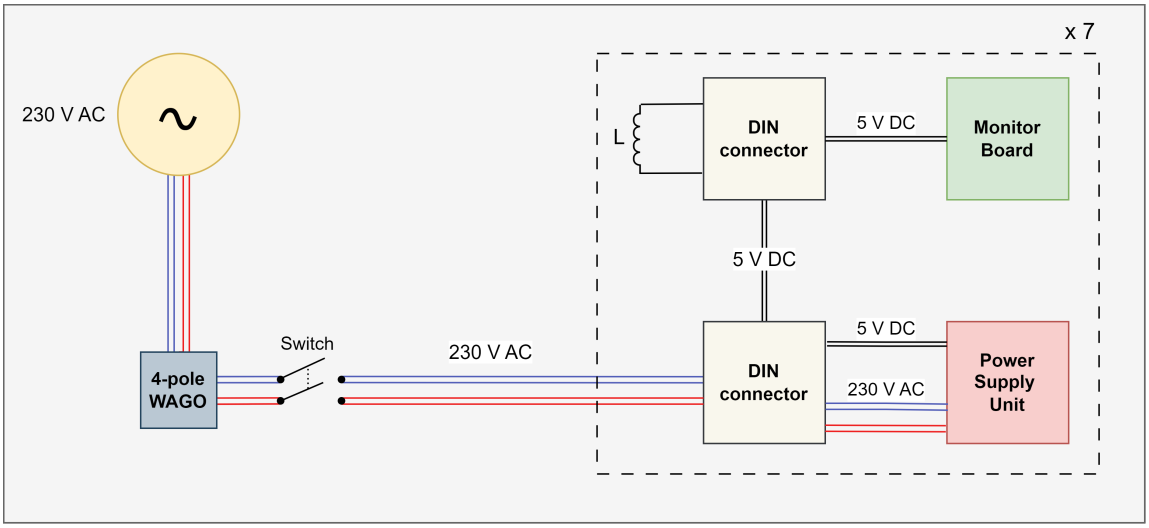

Figure 4.20: Backplane block diagram

4.2.2 Form factor

In order for the backplane to fit into a standard 19 inch subrack with height 3 U (units), it needs to accomodate a maximum width of 84 HP, which equals $84 \cdot 5.08\,\text{mm} = 426.72\,\text{mm}$, and a height of $128.55 \pm 0.15\,\text{mm}$ [21][22]. These measurements are edge to edge measurements.

4.2.3 Connectors

The power connectors which feed AC to the PSUs, and Direct Current (DC) from the PSUs to the MBs, are the DIN 41612 connectors of type H15. The backplane will house the straight connection version, while the MB will use the 90°, right-angle one. This means that the connector on the MB will be able to slot directly into the corresponding connector on the backplane.

The current rating on this DIN-connector is 15 A, meaning that for routes where the possible current draw is greater than 15 A, two or more pins will have to be utilized.

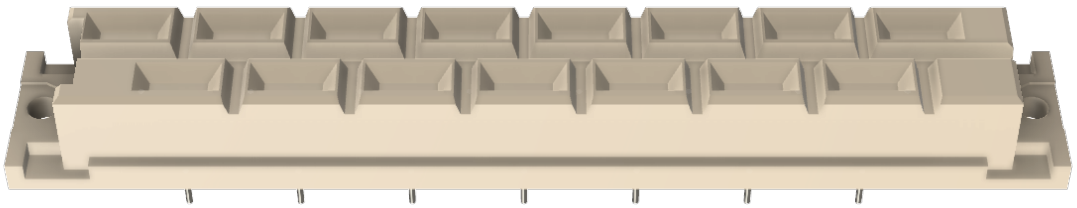

Figure 4.21: DIN41612 connector - type H15 [23]

4.2.4 Current carrying considerations

In order for the backplane to handle high currents, we need to make tracks and planes that are wide, and/or thick enough, to support the current load.

Making a compromise between the PCBs current carrying ability, and the cost of manufacturing, the design involves a copper thickness of 2 $ounce/ft^2$, equivalent to 70 µm, which is twice the standard thickness used in most low-power PCBs, like the Monitor Board.

For the backplane, there are two types of tracks of interest with regards to capacity:

1. Tracks and planes carrying the supply current, rated at 1.6 A, to the PSUs. Since seven PSUs will be supplied by the same track, the current totals to $7 \cdot 1.6\,\text{A} = 11.2\,\text{A}$.
   This applies to the tracks running from the seventh PSU to the wago-connector, and the tracks between the wago-connectors (see Figure 4.22).

2. Tracks and planes carrying up to 16 A at 5 VDC.
   This applies to all the tracks between the connectors for the PSU and MB in each pair, as well as the tracks through the common-mode chokes sitting on the back of the backplane (see Figure 4.22 and 4.23).

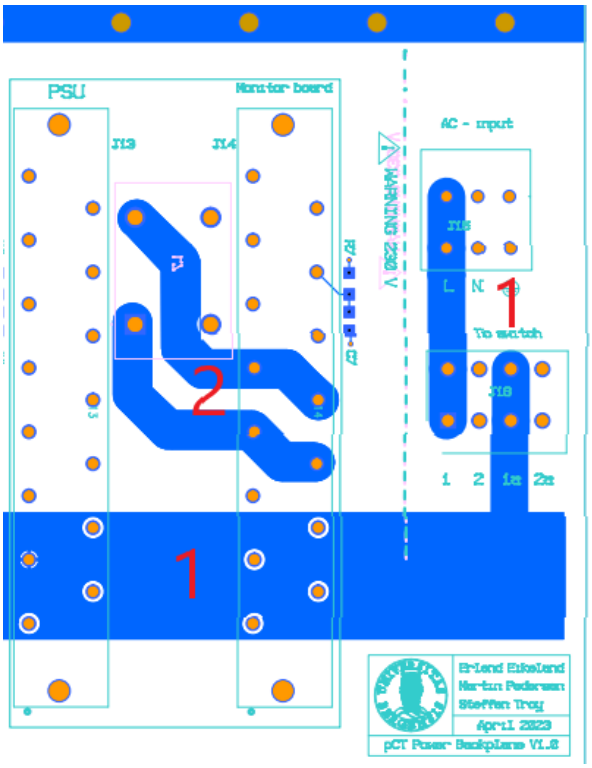

Figure 4.22: Snippet from layer 1 on the backplane

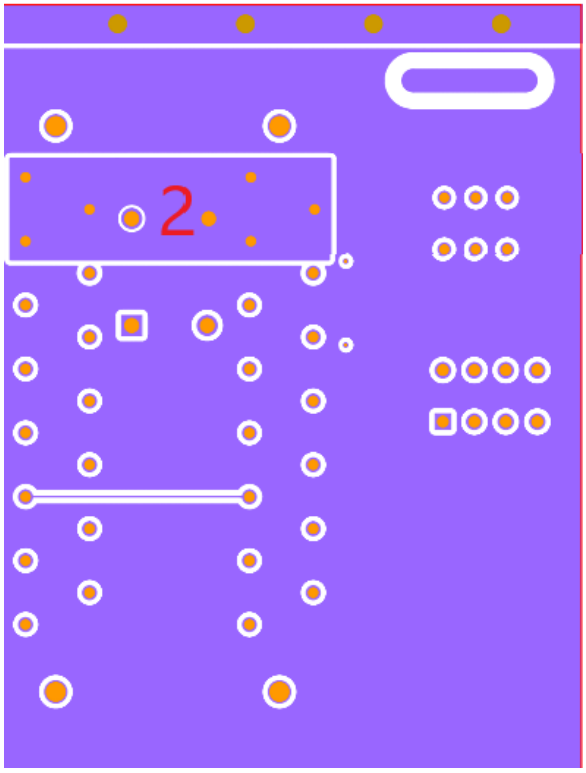

Figure 4.23: Snippet from layer 6 on the backplane

In order to account for worst case scenarios and avoid undersizing the tracks, the calculations do not take into consideration any present copper planes, which would help with thermal dissipation and thus increase the tracks' capacity. The calculations also target a maximum allowed temperature rise of 20°C, whereas in reality, the temperature of the tracks can increase to 30-40°C over ambient without causing a problem. The last buffer for the calculations is that the current draw and delivery of respectively $7 \cdot 1.6\,\text{A} = 11.2\,\text{A}$ and 16 A are **maximums** according to the MAX105 PSU.

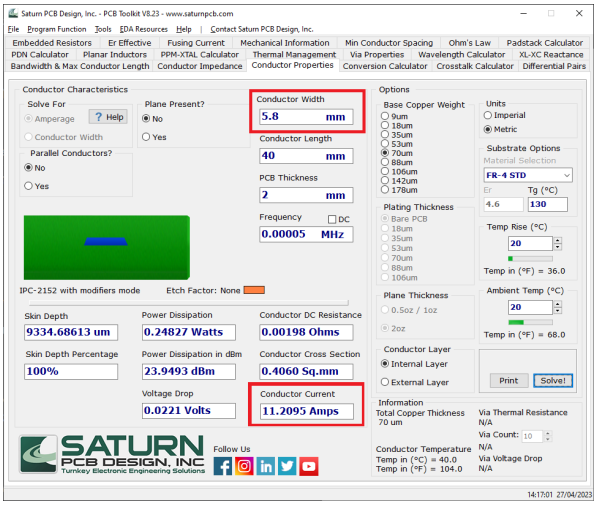

Figure 4.24: Required width for 11.2 A. Screenshot taken from [19].

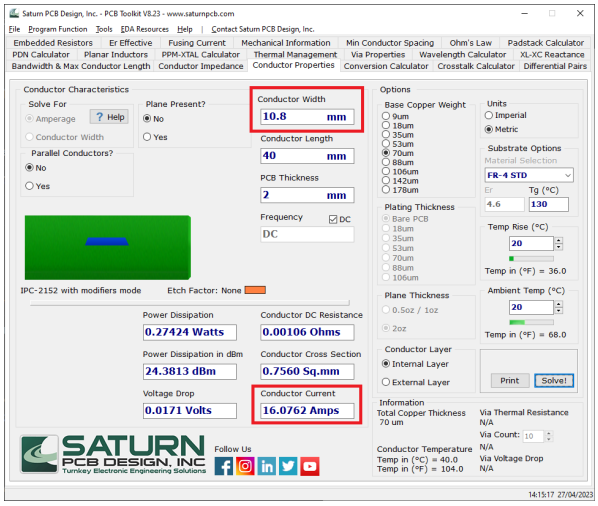

Figure 4.25: Required width for 16 A. Screenshot taken from [19].

As shown in Figure 4.24, the required width to give enough capacity for 11.2 A is ≥5.8 mm. In our layout, we have opted to use 6 mm wide tracks. Coincidentally, this is close to the maximum available width between the pins of the wago-connectors, which is 4 mm. Continuing with Figure 4.25, the required width to accomodate 16 A is ≥10.8 mm. This causes a problem due to there not being enough space between the pins of the DIN41612-connector for tracks that wide. The simplest solution to this problem, is to put identical tracks on top of each other on separate layers. Using a width of 6 mm, accross both layer 1 and layer 2, we achieve a total width of 12 mm.

In areas where space is not an issue, we have put significantly wide copper planes; For the 5 VDC-planes going directly between PSU and MB, the copper plane is 16 mm wide, and the planes carrying 230 V longitudinally across the PCB to supply all the DIN41612-connectors are 20 mm wide.

4.2.5 Grounding and ground coupling

Chassis ground on the backplane, which could also be called AC ground, connects to ground on the AC-input cable, as well as to the chassis on the rack through the mounting holes for the PCB. All the mounting holes, located along the horizontal edge of the PCB, are connected to the chassis ground-net. To aid with electrical connection to the metal on the rack, a 6 mm-wide strip of bare copper, also connected to the ground-net, is laid across the mounting holes as shown in Figure 4.26.

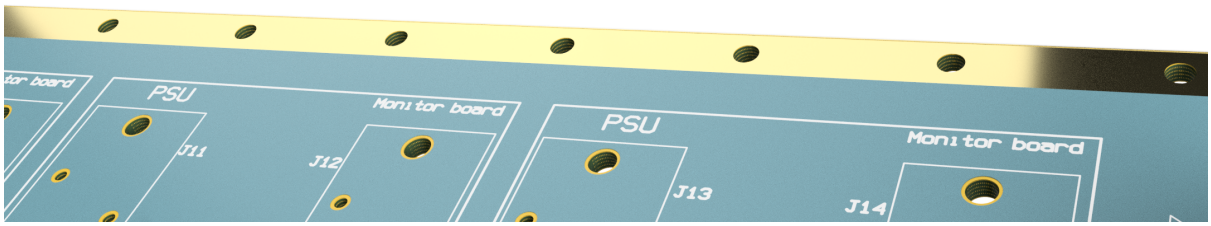

Figure 4.26: Copper plated edges

In addition to chassis ground, there are also seven signal ground nets, one for each pair of MB and PSU. The signal ground nets are AC-coupled to the chassis ground through a 1 MΩ resistor in parallell with a 0.1 µF capacitor, as detailed in Figure 4.27. In this way, if any charge is gathered in one of the signal ground nets, it can be discharged immediately through the chassis ground.

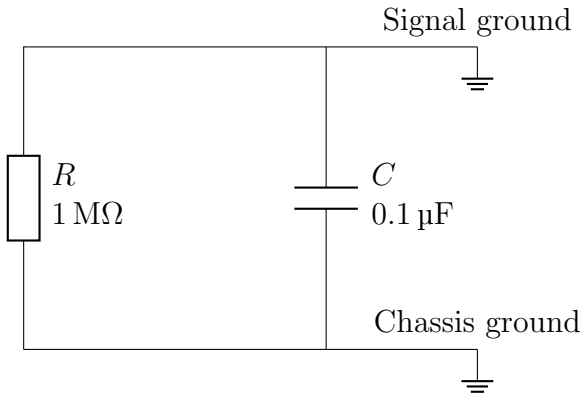

Figure 4.27: Coupling between ground domains

In the early phase of the project, one of the decisions to be made was wether or not the 5 V VDD lines supplying the MBs should be separate. The MAX 105 power supply has a current sharing mode, which would enable the seven power supplies per backplane to work together in delivering the current to the ALPIDEs. This has the advantage that if the current draw from the ALPIDEs is ever too much for one PSU to handle, the others can share some of the load. This idea ended up being declined due to the potentially catastrophic short circuit current of $7 \cdot 16$ A.

4.2.6 Metal balancing

A problem which may arise especially when dealing with large-size circuit-boards is that if the distribution of copper throughout the layers is uneven, the PCB can bend in favour of whichever side of the card that has more metal. Figure 4.28 illustrates an exaggeration of this effect for a two-layer card in which one of the layers is more heavily populated with copper than the other. Bending or warping happens during manufacturing, due to the temperature and pressure of the manufacturing process [24].

Figure 4.28: Warping as a result of copper imbalance

To counteract this effect on the backplane, some counteractive measures have been used:

- Copper-heavy layers are placed as "opposites" in the stackup. This implies that they are even about the center of the card. The two chassis ground-planes (which are full of copper from end to end) are placed on respectively layer three and four in the six-layer stackup.

- Metal balancing, also known as copper balancing, is used to create balance in the remaining layers. I.e. if layer one has plenty of copper on a specific spot, but layer six (its "opposite") does not, layer six will have Not Connected (NC)-copper put in the same spot.

Xpedition Layout's "Metal balancing processor" [25] has been used for this purpose, allowing us to flood all the remaining layers with copper throughout. This ensures that the copper should be balanced, as all areas of every layer will have copper, and we get the added benefit that the PCB will be more robust thanks to more metal.

4.2.7 Stackup

A few considerations were highlighted along with the decision of how we wanted the stackup for the backplane to be:

1. The power delivery tracks of 230 V (called Power L and Power N in the stackup) and 5 V (called VDD) are separated as much as possible.

2. In accordance with the metal balancing discussion in Section 4.2.6, the two edge-to-edge chassis ground planes should be on opposite sides about the center of the stackup.

3. Signal ground should be adjacent to VDD.

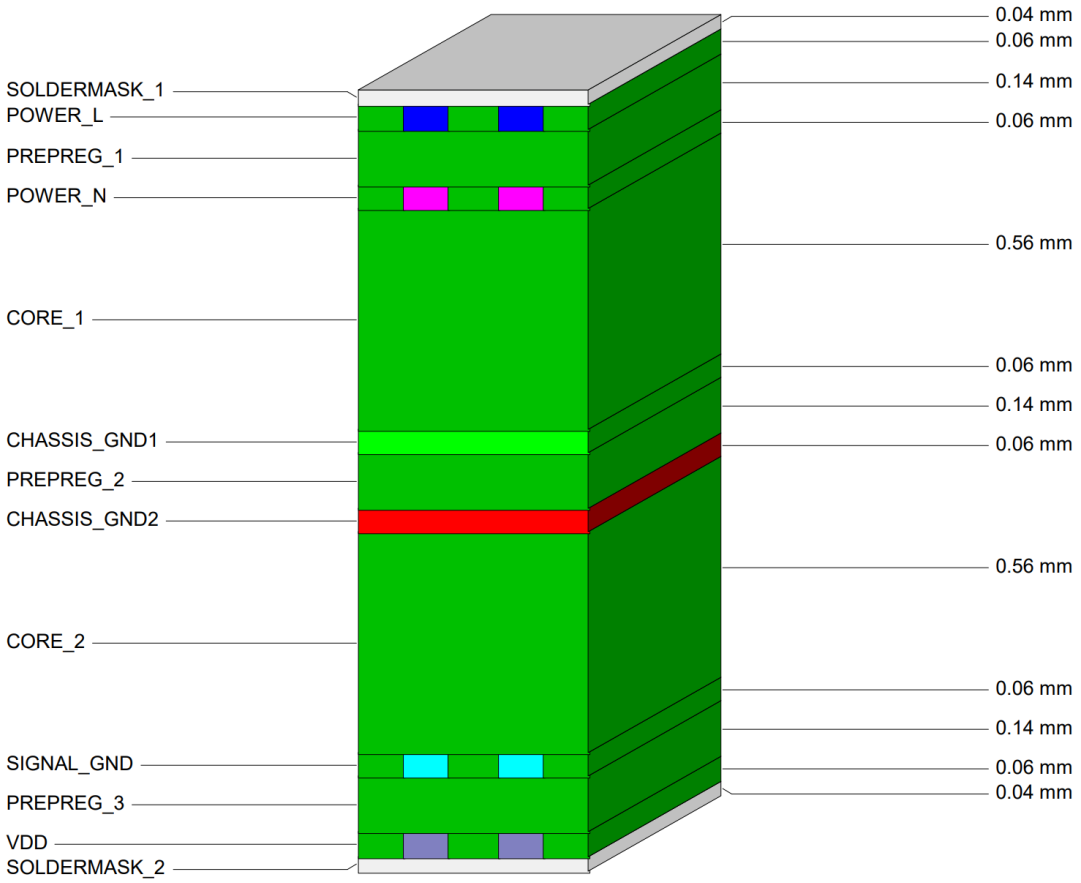

Figure 4.29: Backplane stackup

The stackup is shown in Figure 4.29. By having high and low voltage on opposite sides of the chassis ground planes and two thick cores, the VDD-layer is well protected from the high voltage of the Power L and N layers.

4.2.8 Power switching

One of UiBs requests regarding the rack solution was to be able to turn the power to the PSUs on and off without having to disassemble the rack or having to reach towards the backplane with your hands and thus being at the risk of touching a high voltage pin. Implementing simple functionality through a WAGO-connector allows for a 2-pole switch to be mounted at the front panel for easy access.

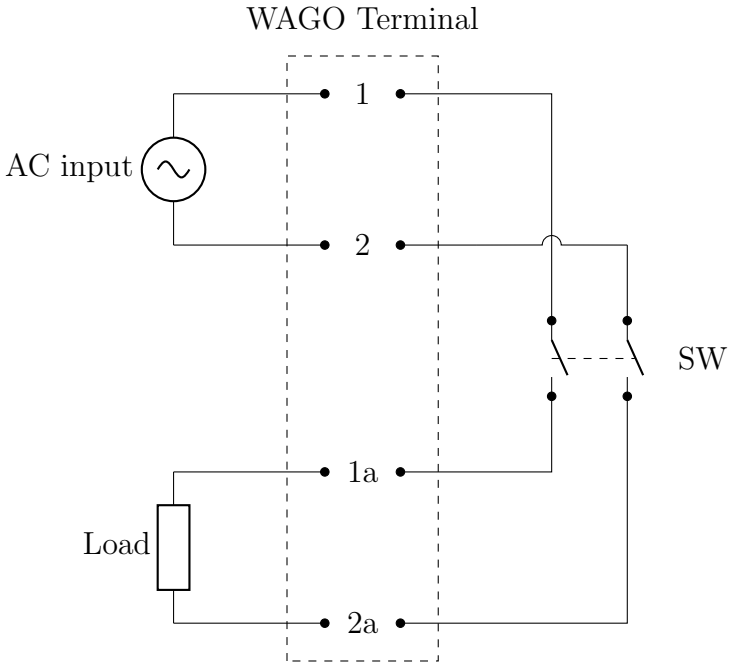

Figure 4.30: Switch wiring

Figure 4.30 shows the schematic of how the switch is wired. "AC input" represents the other 3-pin WAGO terminal where AC power is input, whereas "Load" represents the power L and power N planes going to the PSUs.

4.2.9 Issue with the input ripple filter

As briefly mentioned in Section 4.1.2, due to having to replace the common mode choke in the ripple filter for the DVDD-line with a significantly larger inductor, the choke is now placed on the backside of the backplane instead of on the MB. As shown in Figure 4.31, this has been implemented by connecting the choke to 5 VDC and signal ground directly on the backplane, and feeding the filtered DVDD and Digital Ground (DGND) to the MB through available pins on the DIN41612-connector.

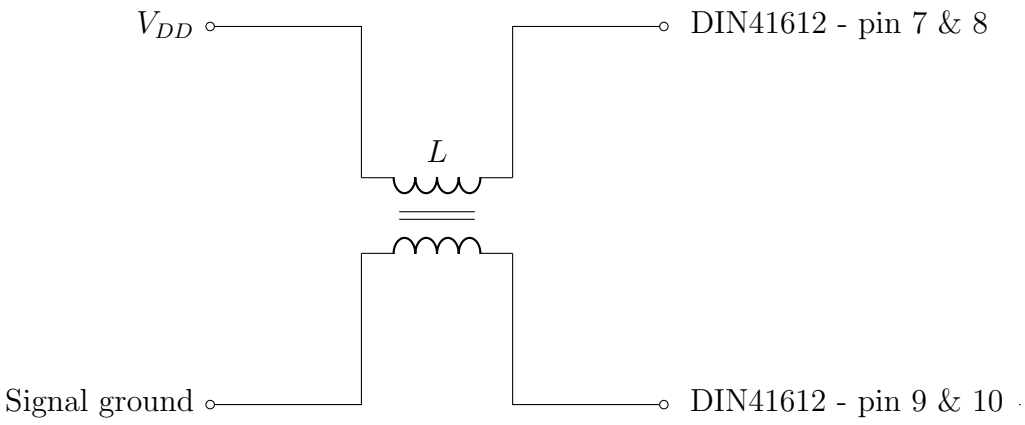

Figure 4.31: Inductor for the ripple filter sitting on the backplane

During high-speed testing at UiB, strings in a 12-string layer were registered to draw 880 mA of digital current consumption [4], totaling $12 \cdot 880\,\text{mA} = 10.56\,\text{A}$ for a whole layer. The pins on the DIN41612-connector are rated for a maximum current of 15 A, meaning that, in theory, one pin is enough to transfer the DVDD-line. However, we have more available pins on the connector and see no point in not proofing the design towards higher currents. Hence DVDD uses pins 7 and 8, while DGND uses pins 9 and 10.

4.2.10 Design Revisions

As mentioned later in Table 5.2, Section 5.5 for testing of the backplane, two initial design errors were discovered:

The silkscreen labeling for the WAGO-connector for the switch is wrong. In our prototype we have labeled the pins from the mains input pin "1" and "2", and the pins for the load pin "1a" and "2a", see Figure 4.30. Having it this way means that the LED on the switch is turned on while the switch is disconnected, and turned off while the switch is connected. The other way around is correct.

Due to the mounting holes on the DIN-connector used by Birger Olsen in his old monitor board prototype not fitting the holes in his PCB, we initially thought there was an error on the footprint for the DIN-connector. Our solution to this was to edit the footprint and offset all the holes except the mounting holes by 100 mils (2.54 mm). However when we ordered the card and the components and tried to mount the connector, we realized that the connector that Olsen had used for his prototype was not the same as the one he had specified in his bill of materials (which is the one we have ordered and need to use). Hence, when we edited the footprint, we did so based on looking at the wrong connector. As a result, the mounting holes on the DIN-connector on our prototype do not fit the holes in the backplane. In fact, if we had not made any changes to the footprint initially, it would have fit. Now we have to edit the footprint again and move the holes back to where they were originally.

Later on in the system test in Section 5.6, a third error was found:

The DIN-connector for the PSU and the MB is supposed to be connected 1-1, 2-2 ... 15-

15. However, when done this way on our prototype, with the way the MB is inserted, it reverse connects to 1-15, 2-14 ... 15-1. This way, the VDD output from the PSU connects to ground on the MB, instead of VDD. As a result, we have to flip the connection between PSU and MB on the backplane in order to connect them together for the system test. In a future revision for the backplane, this error needs to be resolved by connecting them 1-15, 2-14 ... 15-1 in the schematic, as we have done with external cables in our system test. This has been corrected in the new revision of the backplane.

4.3 Microcontroller software

The microcontroller software was rewritten from the ground up, this was done to create a more modular and reliable system. The software is written in C and C++ and implemented using the PlatformIO extension for Visual Studio Code. This extension allows for easy compiling of the code along with a simple and easy to use debugger. The code was written with modularity in mind, where each of the microcontroller modules used, has its own source and header file, along with a documentation file to describe the functionality. This should make it easier to maintain and update the code in the future.

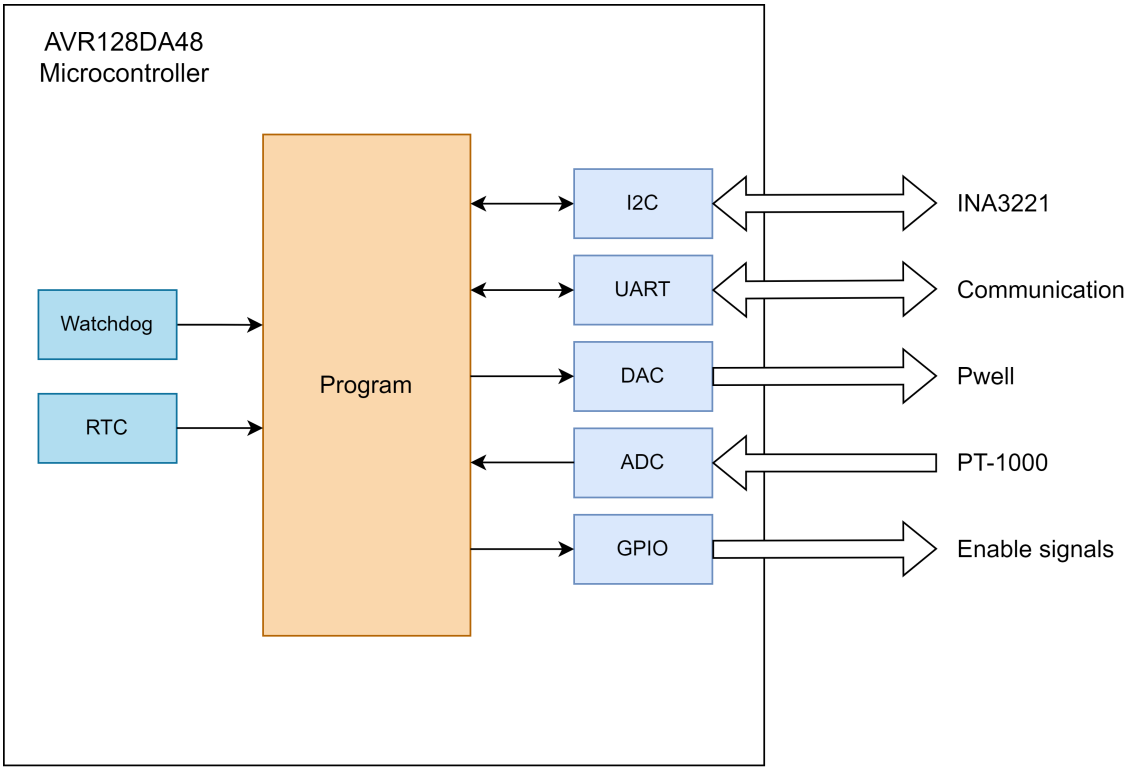

Figure 4.32: Overview of microcontroller software

4.3.1 Watchdog timer

In autonomous system design, it's crucial to anticipate and prepare for unexpected errors that may occur during runtime. One effective method for addressing this concern is through the use of a watchdog timer. The AVR128DA48 microcontroller has an internal watchdog module, this is a timer that runs continuously and can be configured with a specific timeout period. If this timer is not reset by the software within the designated time frame, it will automatically issue a system reset. This functionality allows the

microcontroller to recover from uncontrolled or deadlocked code, ultimately improving system reliability and performance.

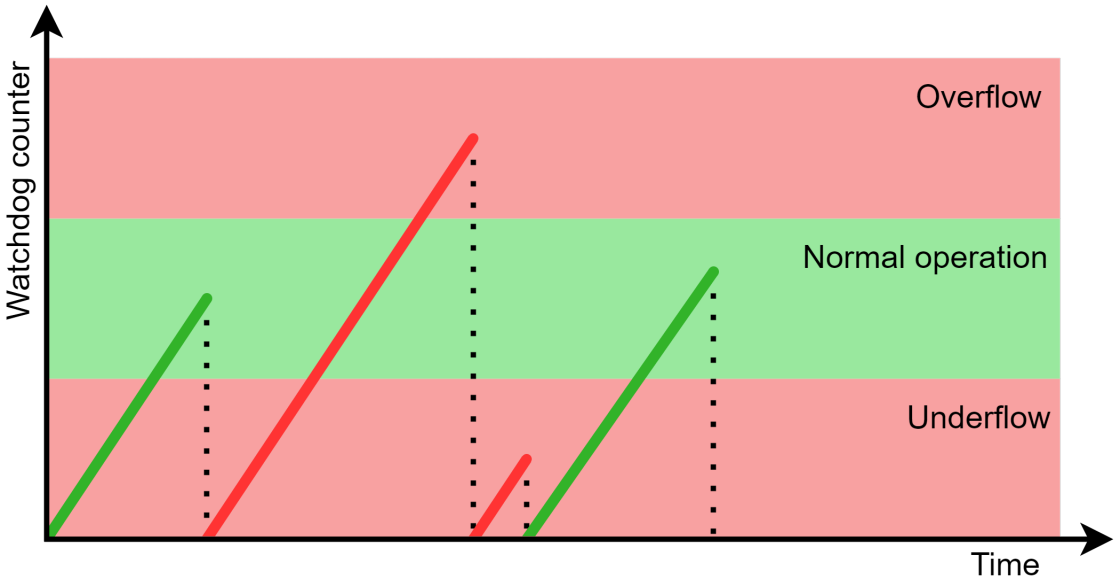

Figure 4.33: Windowed mode watchdog timer

The watchdog module is able to operate in either a windowed or a normal mode. In windowed mode, the watchdog timer must be reset within a specific time window. If the timer is reset outside of this window, meaning before or after a specific period, a system reset is issued. In normal mode there is only an upper limit on the time window, meaning it can be reset at any time before the timeout period expires.

For our use the normal mode of operation is used. Since the watchdog is never reset inside a for or a while loop, it can never be reset too early. In our design the timeout period is set to 2 seconds, this assures that all operations should be completed before the watchdog timer expires and the system is reset.

4.3.2 Communication

The AVR128DA48 has several built-in UART modules, one of these are used for serial communication between the microcontroller and the MB hub. Each of these modules has their own fractional baud rate generator, the signal generated is derived from the internal high-frequency oscillator with a maximum frequency of 24 MHz. The baud rate is calculated using the following equation:

$$Baudrate = \frac{64 \cdot f_{CLK\_PER}}{S \cdot BAUD} \tag{4.1}$$

Where f_{CLK_PER} is the frequency of the internal high-frequency oscillator, S is the number of samples per bit and $BAUD$ is the value of a 16 bit register, which is to be modified depending on the baudrate needed. The number of samples per bit is either 16 or 8 de-

pending on whether the UART module is in normal or double-speed mode. The maximum baud rate is therefore 1.5 Mbps for normal mode and 3 Mbps for double-speed mode.

When going from normal to double-speed mode the baud rate is doubled, but the number of samples used for data sampling and clock recovery is halved. This means that the baud rate setting needs to be more accurate and the peripheral clock needs to be more stable. Since the peripheral clock is derived from the internal high-frequency oscillator, which has a frequency accuracy of ± 2% [13]. We decided to use the normal mode of operation, since error tolerance is more important than speed.

UART protocol

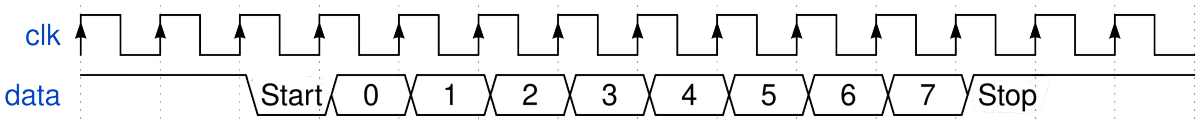

Figure 4.34: UART frame

As seen in Figure 4.34, the UART frame used by the microcontroller consists of one start bit, 8 data bits and 1 stop bit.

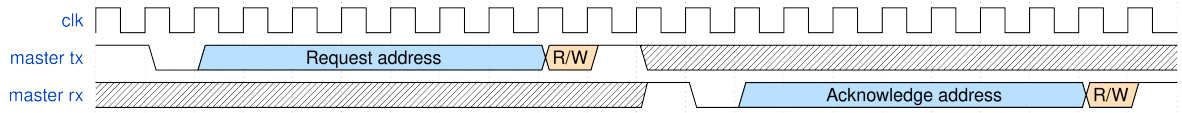

Figure 4.35: UART request from master to slave

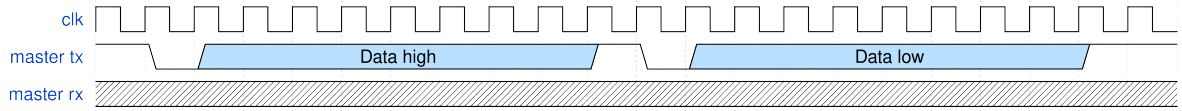

Figure 4.36: UART write operation

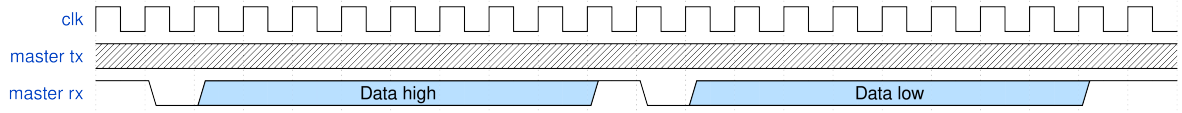

Figure 4.37: UART read operation

As shown in Figure 4.35, the protocol for communicating with the microcontroller is fairly simple. The microcontroller acts as a slave and a master can initiate a read or a write operation to a 7-bit address. If the address is a valid read/write address, the slave will respond by transmitting the same address back which acts as a handshake between the master and the slave. Depending on the R/W bit, the microcontroller can either receive 16 bits of data (Figure 4.36) or transmitt 16 bits of data (Figure 4.37). Each of these operations are sent in 2 UART frames as seen in Figure 4.34, adding up to a total of 2 bytes of data either sent or received. Of these two bytes the 8 most significant bits are sent first.

UART interrupt handler

To save processing time and power, UART interrupts are used in combination with a buffer. This allows the microcontroller to continue with other tasks while waiting for a new request. When a new interrupt is triggered the data is immediately stored in the buffer, allowing the microcontroller to process this new data when it is ready.

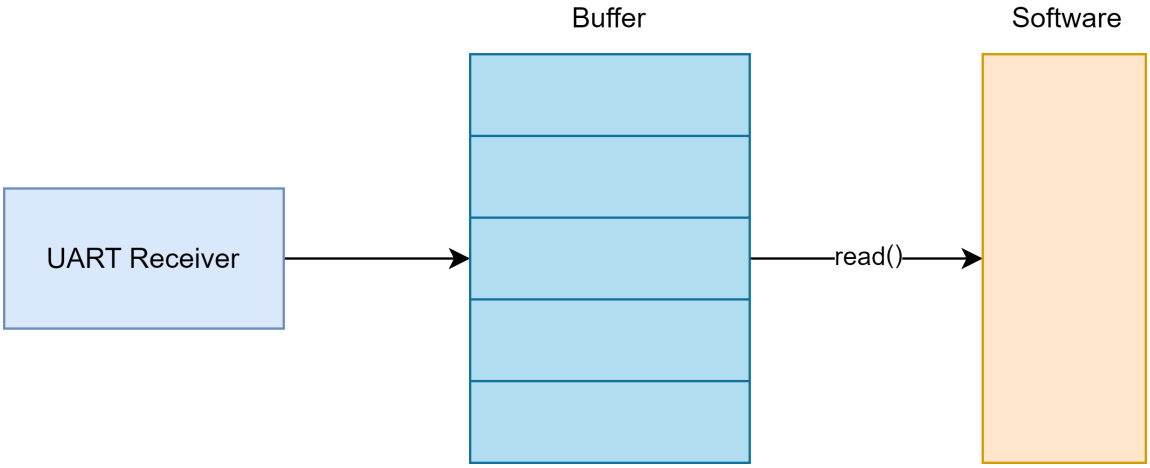

Figure 4.38: UART receiver buffer

As seen in Figure 4.38, the program can use the read() function to check if there is new data available in the buffer. If there is new data available the function will return the data and remove it from the buffer. If not, it will return -1. This allows the program to continue with other tasks instead of polling the UART module for new data on each iteration of the main loop saving both time and resources.

4.3.3 Current monitoring

One of the most important aspects of the microcontroller is to be able to monitor the current and voltage draw of the AVDD, DVDD and PWELL lines. As described in Section 4.1.6, this is done using Inter-Integrated Circuit (I2C) communication between the microcontroller and the INA3221 chip.

The microcontroller is able to read and write to a set of register inside the INA3221 chip. By using the real-time counter module featured inside the microcontroller, the program is able to periodically fetch new data from the INA3221 chip. This fetch period is adjustable and can be set by writing to the RTC_PERIOD_ADDR register.

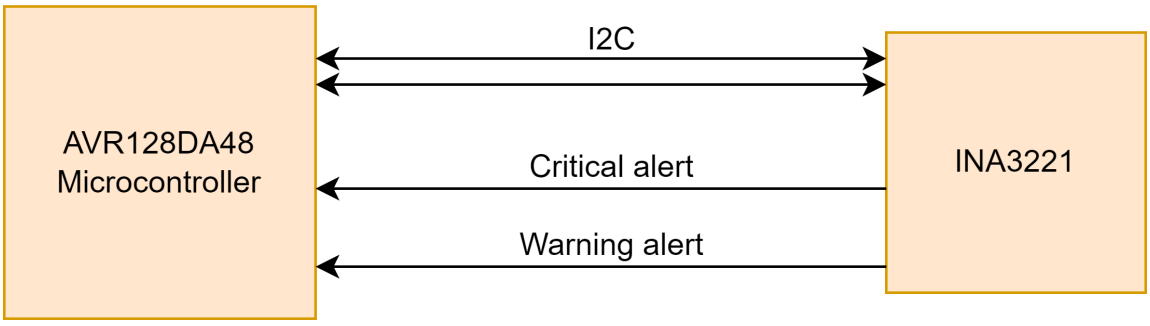

Figure 4.39: Microcontroller connection to INA3221 chip

In addition to the I2C connection, the INA3221 chip connects to the microcontroller with two other signals. These are the critical and warning alert lines. These lines will drop from high to low voltage when the set current/voltage threshold values is exceeded. These lines are connected using a interrupt which when triggered by the warning line will set a new error in the error register. If the critical line is triggered, the microcontroller will disable all enable lines turning off the power to all of the chips connected.

The INA3221 chip establishes a connection with the microcontroller through the I2C interface, as well as two additional signals known as the critical and warning alert lines. Whenever the current/voltage threshold values are surpassed, these lines transition from a high voltage level to a low voltage level. To integrate this functionality in the code, a interrupt is set to trigger on these lines. Once the warning line triggers the interrupt, a new error is recorded in the error register. On the other hand, if the critical line is triggered, the microcontroller takes action by disabling all enable lines, resulting in the power being turned off for all chips connected.

4.3.4 Temperature monitoring

The PT-1000 circuit has remained the same as on the previous board, leaving us with the same calculations for the incoming PT-1000 voltage range as on Birgers board, where 0 to 100 °C which is mapped to the voltages 0.417 to 0.542 V, [8, p. 66]. To read this voltage the built-in 12 bit ADC module is used. In the previous version the ADC reference voltage was set to 2.5 V, but to get a higher resolution reading we lowered the reference voltage down to 1.024 V, this gives us a resolution of 0.25 mV. Which means that we are able to detect a change in temperature every 0.2 °C.

4.3.5 Pwell voltage generation

The same pwell voltage amplifier with a gain of -3 is used on the new board as on the previous board. This means that the output voltage needed still needs to be in the range 0 to 2 V. To do this the Digital-to-Analog Converter (DAC) module of the microcontroller is used. The pwell circuitry is really sensitive, so to get the output voltage as accurate as possible we lowered the reference voltage of the DAC from 2.5 V to 2.048 V. This means that we are able to generate a output voltage from the microcontroller with a resolution of 2 mV and a output voltage from the MB with a resolution of 6 mV as it is amplified by a factor of -3.

4.3.6 Registers

The communication described in Section 4.1.4, is used to read and write data to a set of registers inside the microcontroller. the master can send a request to a 7 bit address. This gives us a total of 128 potential addresses, But as most of the values we want to read/write are more than 8 bits long, we combine two registers to form 16 bit registers leaving us with a total of 64 addresses. A complete address map can be found in Appendix A.1. The registers are divided into 3 categories, normal registers, control registers and error registers.

4.4 FPGA design

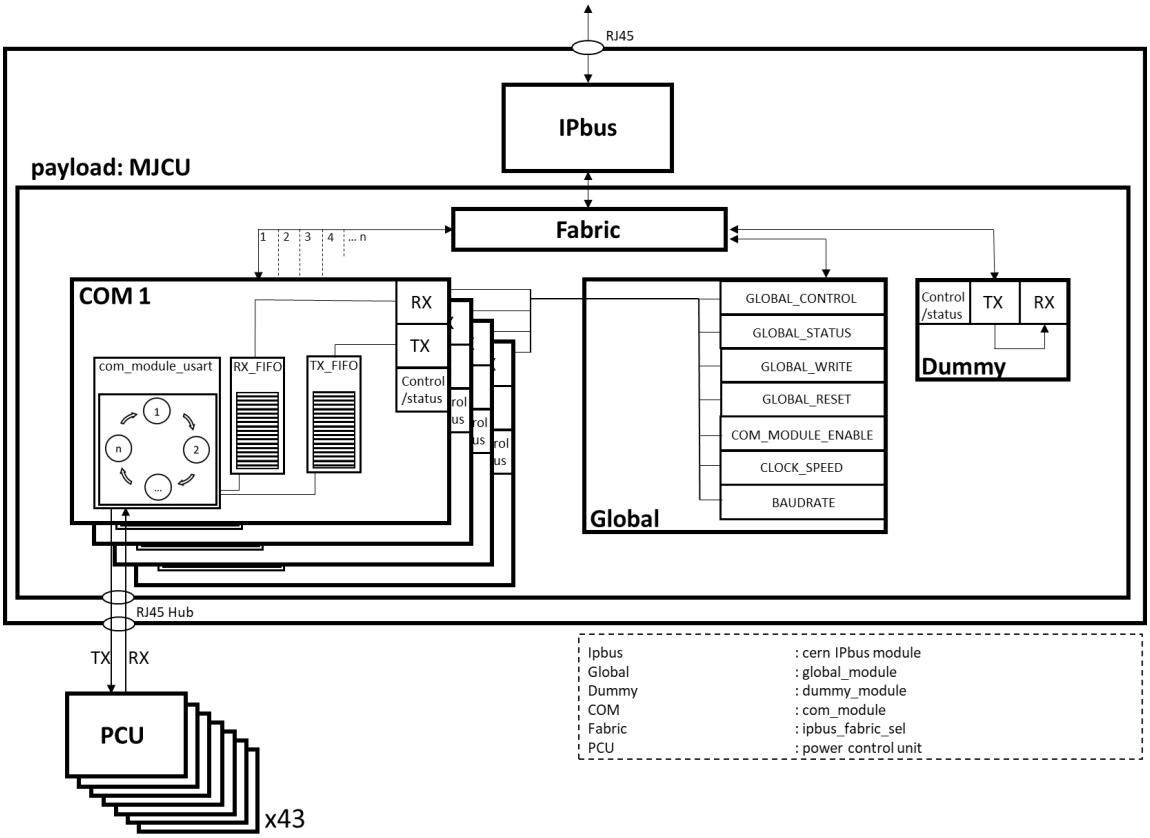

Figure 4.40: Previous FPGA design. Illustration taken from: [11]

The previous design shown in Figure 4.40 was done by Martin Eggen and Jakob Hauser as their bachelor thesis [11]. As this design was designed to work with the previous MB, the old USART protocol was still used. To accommodate to the new design, the UART module needed to be redesigned.

4.4.1 New UART design

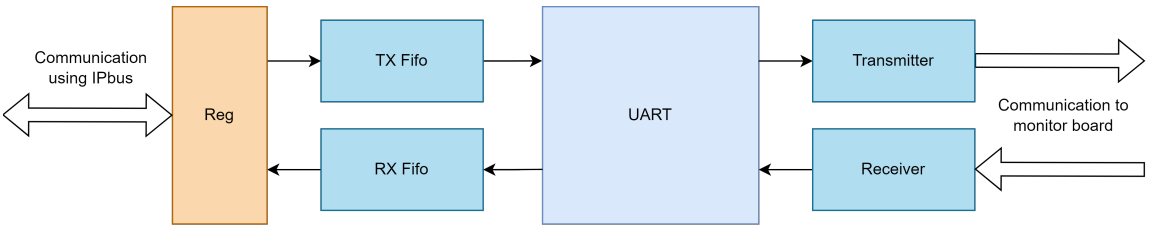

Figure 4.41: Implementation of the UART module

The new design still uses IPbus [12] as communication between the MB hub and the control room, the IPbus can write to one First In First Out (FIFO) and read from another FIFO. These FIFO's are then connected to the UART module, allowing the MB hub to send and receive data from the MB.

The previous design utilized a single VHDL entity for both transmitting and receiving data. In the new version it was changed to use two distinct files, one for transmitting and the other for receiving. The motive behind this alteration was to enhance the code's modularity, the two entities are linked in a top-level file, which connects them to the FIFOs.

To make the UART receiver and transmitter more modular the two entites use a file called uart_pkg.vhd, which is a VHDL package file containing a custom UART config type. This can be changed to allow for a different UART config to be used. In our case this was set to 8 data bits, 1 stop bit and no parity bit, to match the UART frame used by the MB described in Section 4.3.2.

UART top level

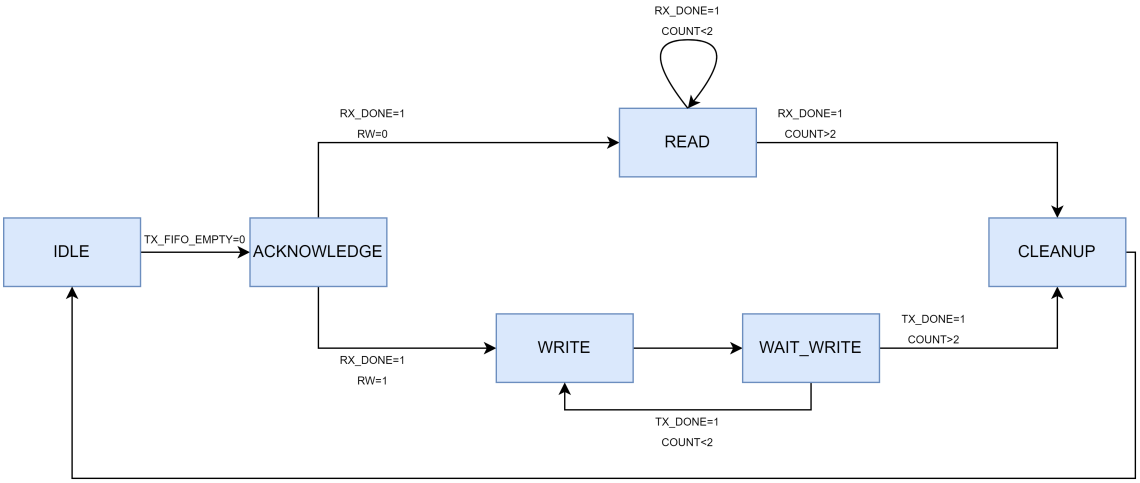

Figure 4.42: UART state machine

The UART is implemented using a state machine, which waits in an IDLE state until the transmission FIFO no longer is empty. Depending on the RW bit either a write or a read operation is then issued. Both the transmitter and receiver uses a done signal to tell us when the module has excecuted the current operation. These signals are used in the state machine to change to the next state.

In some cases the acknowledge or read data might not come back, as a fault in the MB or communication can occur. This will cause the receiver done signal to never go high resulting in the state machine being stuck. To avoid this, a timeout counter has been used in the states which are dependent on a response from the MB. This allows the state machine to recover from a fault and go back to the IDLE state.

4.4.2 Project based TCL script

When creating a Vivado project there is two main approaches used. The first is to create a project using the Vivado graphical user interface. This approach is simple to use, but is often prone to time consuming errors when the project is imported on a different computer. The second approach is to create the project using a Tcl script. This gives us an automated and repeatable way to create the project which is more robust and less

prone to errors. This method is also beneficial when working in a GIT version controlled environment, as it allows all contributors to use the same project settings. Since this solution gives us alot of flexibility, it is the approach we have chosen to use in this project.

4.5 Adapter Board

This section involves a design sketch for an adapter board which will act as a RJ45 hub for connecting all the monitor boards to the MB hub. Note that this is more of a feasibility study, as opposed to the work done on the monitor board and backplane which are complete designs.

4.5.1 Background

The need for an adapter board as an interface between the MBs and the MB hub arises due to there naturally not existing any development board with 43 available RJ45-ports for inputs from our MBs.

With the design of an adapter board, we can utilize higher pin count IO-connectors on development boards by interfacing between the RJ45 connectors on the MBs and the IO-connectors. Having two LVDS circuits with two pins each, across 43 MBs, we need a total of 172 available IO-pins on the development board.

4.5.2 Block diagram

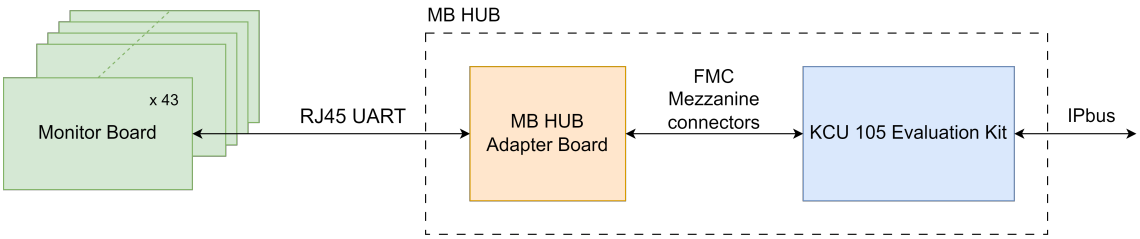

Figure 4.43: MB HUB Adapter Board

4.5.3 Connectivity

The Kintex Ultrascale FPGA KCU105 Evaluation Kit is specifically selected for use in the pCT project. It has two GPIO connectors, one 400-pin high pin count connector and one 160-pin low pin count connector. In total, these offer more than 172 free use LVDS pins [26], meaning that our need for IO-pins is satisfied with just these two connectors. To connect to these, the adapter board simply needs their mezzanine card counterpart.

For connection into the adapter board from the MBs, $\geq$ 43 RJ45-connectors are needed. Contrary to the evaluation board that houses the FPGA, we can design our adapter board to fit as many connectors as we need. Three 16x blocks of connectors gives us the 43 we need, with 5 to spare which can be used if there is a need for more than 43 layers in the calorimeter, or for any other expansion.

4.5.4 Design draft

Figures 4.44 and 4.45 show our proposed design for the adapter board.

Figure 4.44: Top side of the proposed adapter board

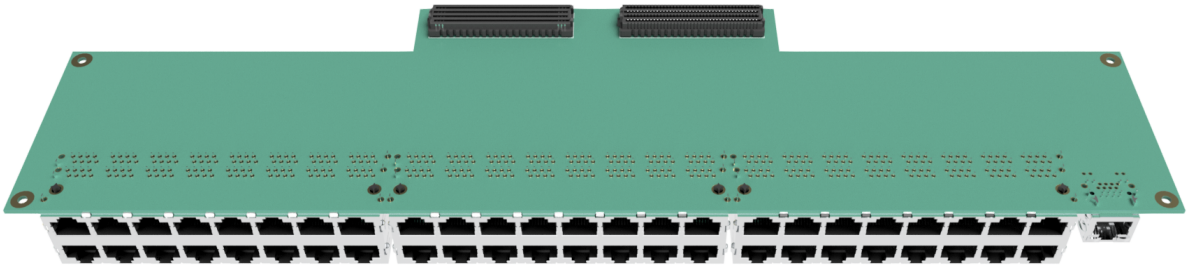

Figure 4.45: Bottom side of the proposed adapter board

To comply with the plan that the equipment be mounted in racks, the adapter board is 400 mm wide, which makes it able to sit attached to the bottom of a 19 inch rack, the same rack width as for the MBs and PSUs. As far as the depth and height for the rack goes, any arbitrary dimensions ≥ 2 units in height and 300 mm in depth is able to fit both the adapter board and the FPGA evaluation kit. This way, all the RJ45 connectors from the monitor boards can plug into the three 16x RJ45 connector blocks in the rack, and the single RJ45 connector can function as output for the IPbus to the computer in the central control room, ref. Figure 3.1.
Figures 4.46 and 4.47 show the intended construction of the adapter board in a rack.

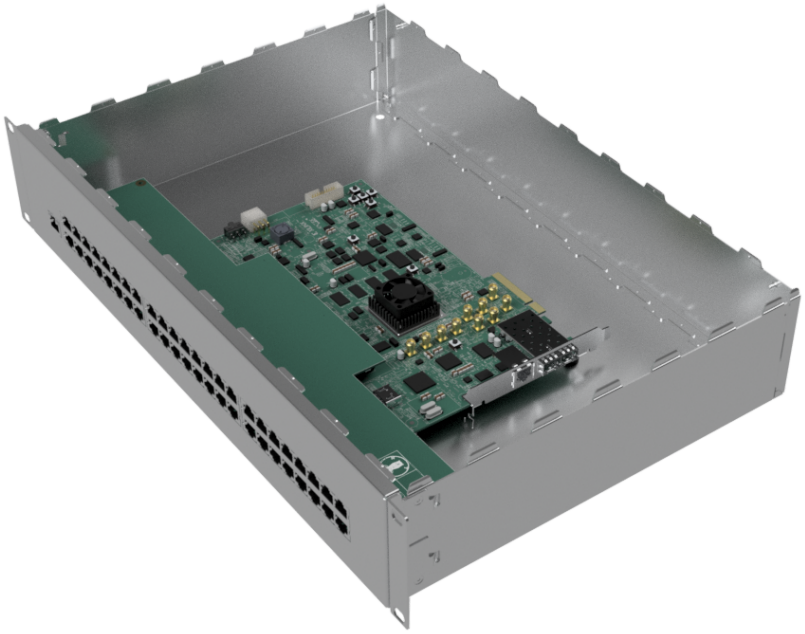

Figure 4.46: Adapter board and rack from the front

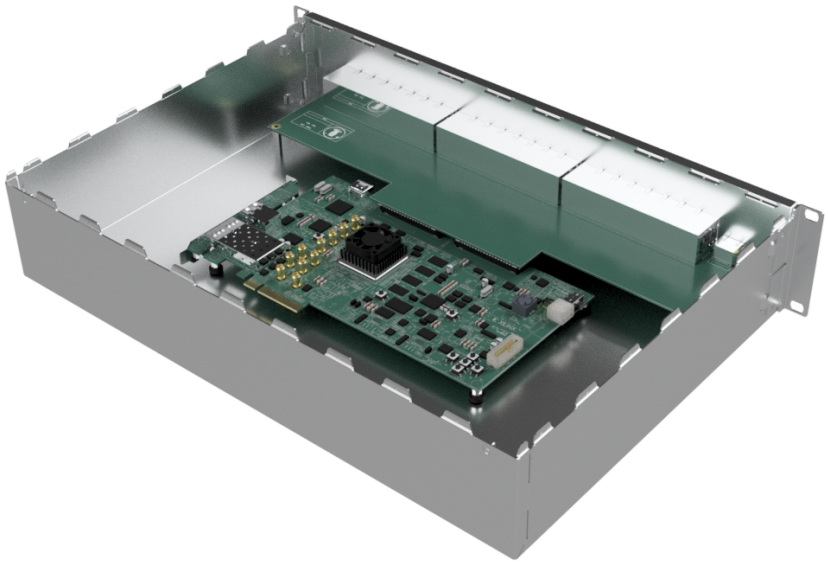

Figure 4.47: Adapter board and rack from the back

4.6 Subrack

The solution we have designed is a subrack which will house up to 7 PSUs and 7 MBs. As each one of these will be able to power a single layer of the TC, this means that a single crate will be able to power up to 7 layers of the TC. With a total of 43 layers total in the experiment, this means that 7 crates will be required to power the entire pCT device.

Figure 4.48: Subrack fully loaded

The subrack is the main component of the crate. It is a 19" rack with a height of 3U and features EMI shielding in the form of grated aluminium plates on the top and bottom, as well as a solid plate on the rear. These grated plates allow air to flow through without letting most of the electromagnetic spectrum pass. The subrack is planned to be mounted in a standard 19" 42U network rack, typically used in modern datacenters and telecommunications.

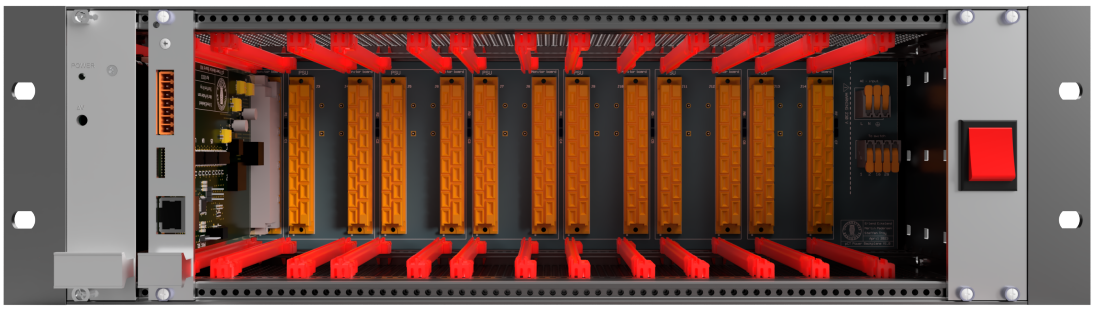

Figure 4.49: Subrack

The rear of the subrack will have a hole drilled in it, and a cable gland will be fitted to protect the AC intake cable from rubbing against the metal case. The subrack itself will also feature plastic rails to allow easy and reliably insertion and removal of the MB and PSU as shown in Figure 4.49.

We have specified that there should be a 6HP wide aluminium front plate in the remaining space in the subrack which can be used to mount the switch to control the power to all the PSUs in a crate at once, without needing to physically disconnect each one or worse, have to unplug the mains cable from behind a fully loaded and wired up network rack.

5 Testing

5.1 Assembly

Both the MB and Backplane were assembled by hand using a soldering iron, hot air gun and flux. The MB was designed to be assembled through the use of Pick and Place technology, but would have been overkill for the manufacturing of a single prototype.

Assembling the MB was difficult through manual tools due to the presence of several components whos pads were underneath and not accessible using common soldering techniques. This poses a serious risk of misalignment, short circuits and bad connections. As such, every PCB must be manually inspected to look for these issues, as well as continuity and resistance measurements to ensure that there are no short circuits and that the components that are difficult to solder do have a good connections.

For future revisions and reorders, a stencil is recommended even for manual assembly. This will greatly reduce the risk of assembly defects and issues. More specifically, this extends to the inductors who have some fairly inaccessible pads on the bottom which requires a fairly powerful heatgun to reflow if an oven or other reflow machinery is not available.

5.2 FPGA verification

Before doing live testing with the FPGA, it's essential to perform simulations to ensure that everything works as intended. Simulations allow for controlled testing in a virtual environment that can replicate the behavior of the system without the risks and expenses associated with physical testing. The FPGA design was therefore thoroughly tested in a VHDL simulation tool called Modelsim. The testbench was written using the Universal VHDL Verification Methodology (UVVM) library, which is a free and open source library for making structured VHDL-based testbenches [27].

The previous work done by Martin Eggen and Jakob Hauser [11], had testbenches for each seperate module of the design, allowing for thorough testing of each component. Since the new design only changed the UART module, alot of the same testbenches could be used to verify the different modules of the design. The main changes had to be made to the dummy MB module which acts as a slave, allowing the design to get stimuli in a simulated environment. By help of the UVVM library we were able to write so called self-checking testbenches, which can verify the design without relying on manual insepection of the outcome.

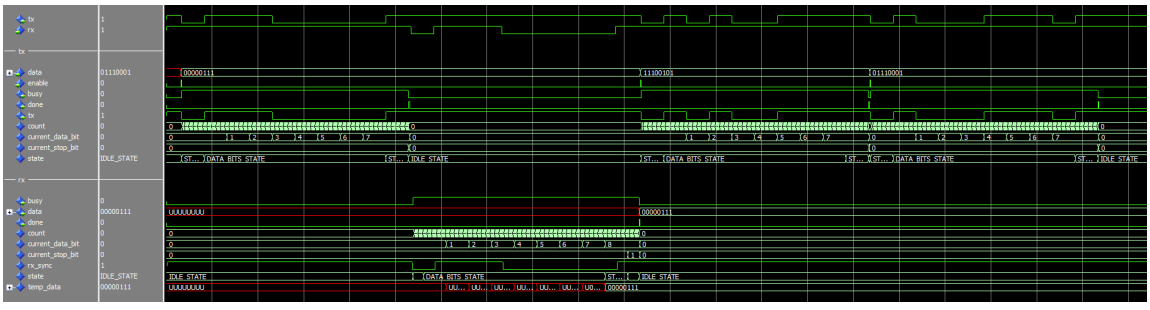

Figure 5.1: Modelsim wave diagram of a UART write operation

Throughout the design process, wave diagrams were also used as they often provide a better and more intuitive way of showing errors or unexpected behavior. The wave diagrams are generated by Modelsim and shows how the different signals behave over time. This is especially useful when testing the UART module, as it allows for easy analysis of the data being sent and received. A example of a wave diagram of a write transmission can be seen in Figure 5.1.

5.3 Monitor Board and software

Test	Criteria/Expected value	Result/Measured value
Verify I2C communication between microcontroller and INA3221 current monitor IC.	Communication should be able to be established, and the values read by the microcontroller should correspond with the register values sent by the INA3221.	See Section 5.4.1 for results.
Verify that the INA3221 critical and warning alert pins are working as expected.	When the current exceeds the critical or warning threshold, the corresponding pin should be pulled low. exceeding the critical threshold should disable all enable pins.	Not tested.
Verify pwell voltage generated.	Voltage generated should have a resolution of 6 mV, and a range of 0 to -6 V as described in Section 4.3.5.	See Section 5.4.2 for results.
Verify temperature measurement.	Read value from the temperature register should within the expected range.	See Section 5.4.3 for results.
Verify enable pins.	All enable pins should be able to be turned on and off, and the pins corresponds to the right pinout.	Enable pins on the MCU side works. Optocoupler has not been verified.
Verify UART communication between the MB and the MB hub.	Communication should be able to be established, and the values read by the MB hub should correspond with the register values sent by the MB. Check for errors in the communication.	See Section 5.4.4 for results.
Verify the reset button is behaving as expected.	The MB is reset.	The MB is not reset. Needs investigation.

Table 5.1: Monitor Board testplan

5.4 Current draw

The MB needed to be verified with the calculations done in Section 4.1.3 to ensure that the PSU can handle the current draw. The current draw was measured with a multimeter, and the results are shown in the figure below. The measurements were done with all the enable pins turned on, and the MCU running in normal operations polling the sensors and sending data over UART.

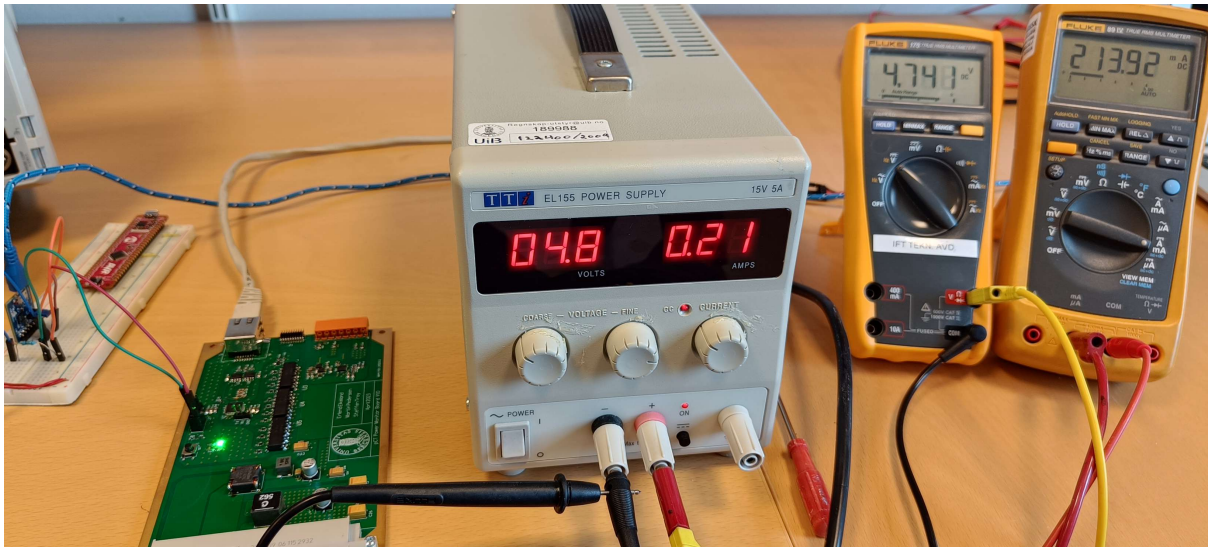

Figure 5.2: Current draw of the Monitor Board

As shown above, the current draw is 213.9 mA at 5 V. This is well within the limits of the PSU. The current draw is even lower than the calculated value in Section 4.1.3 which was at 313 mA.

5.4.1 I2C communication

The I2C communication proved to work without any issues.

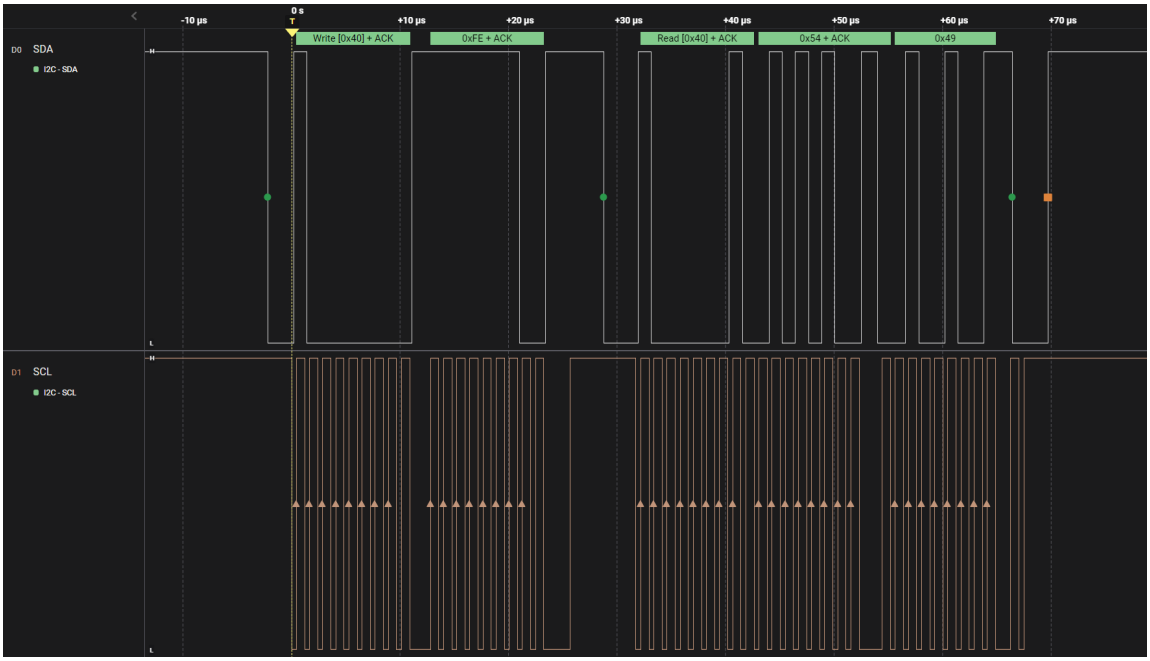

Figure 5.3: I2C Communication

The figure above shows the captured I2C communication where the MCU requests the manufacturer id from the chip. This is a reliable way to verify that its working as the value in return is listed in the datasheet and considered expected behavior.

Further tests show that we are able to read data as expected from the chip, as shown by the figure below that shows the readout of the bus voltage.

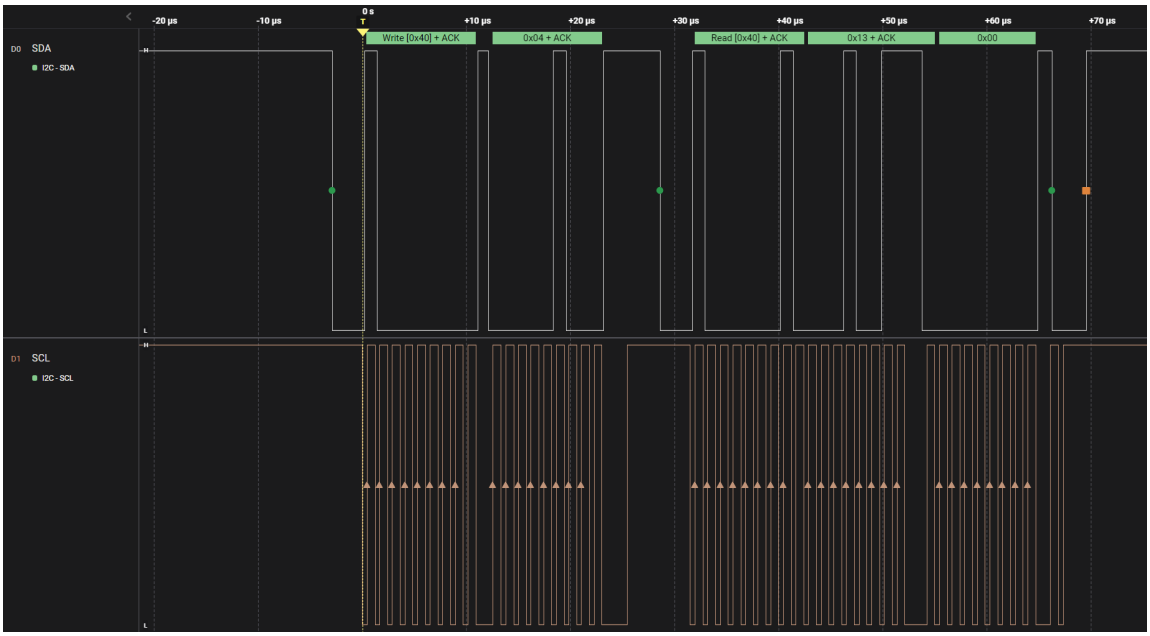

Figure 5.4: I2C Communication, bus voltage

5.4.2 Pwell voltage

Testing showed that the PWELL voltage is not responsive to the software commands sent by a master. Closer inspections revealed that there might be issues caused by assembly.

An attempt was made to fix this issue by resoldering the OpAmp chip, however this did not fix the issue. As the chips markings were not visible enough to determine a proper orientation, another attempt was made where the OpAmp is connected in reverse. This did not fix the issue, and seeminly killed the charge pump. When the chip was off the pads, a continuity test was made to rule out manufacturing defects, where no faults were discovered.

Futher attempts to fix has been halted in order to finish other important tests in time. Replacing the chips all together and verifying the schematic is recommended for future testing attempts.

5.4.3 Temperature measurement

There was no available PT1000 element to verify the temperature measurement design, only a PT100 element was available. This proved a partial success as the MCU was able to read a change in voltage across the PT100 proving that it should work with a PT1000 element.

5.4.4 UART communication

To the test the communication of the MB, it was connected to a computer using a USB to UART converter, this signal was then sent through two LVDS chips. Allowing the front port of the MB to be used.

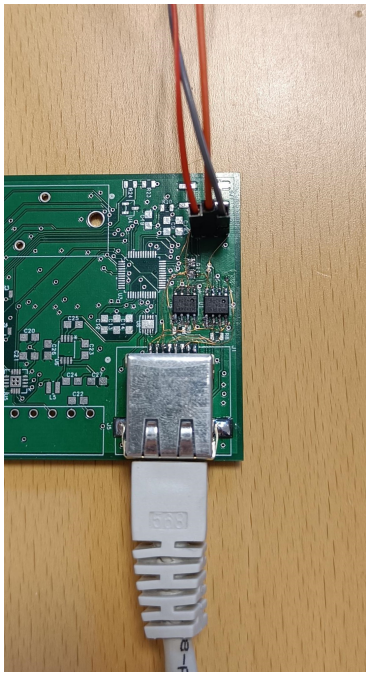

Figure 5.5: USB UART to LVDS

A python script was then used to send a write and a read command to the MB and verify that the data was received correctly. To further verify the data, the Receive (RX) and Transmit (TX) line of the UART was connected to a logic analyzer allowing us to get a visual representation of the data.

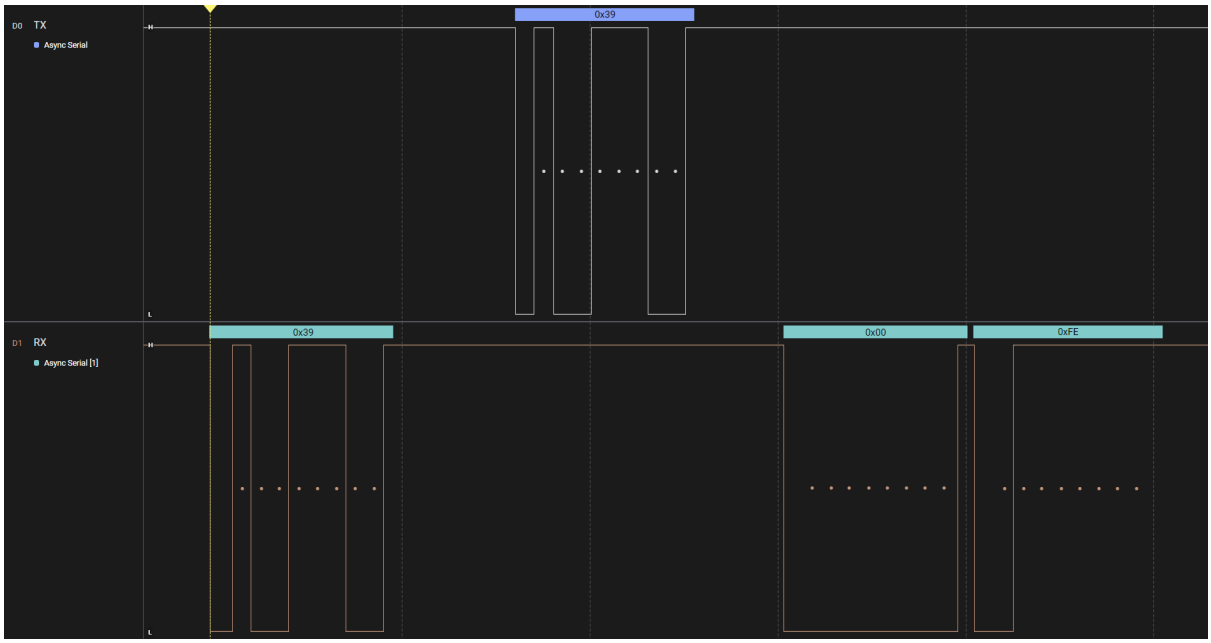

Figure 5.6: Logic analyzer write operation

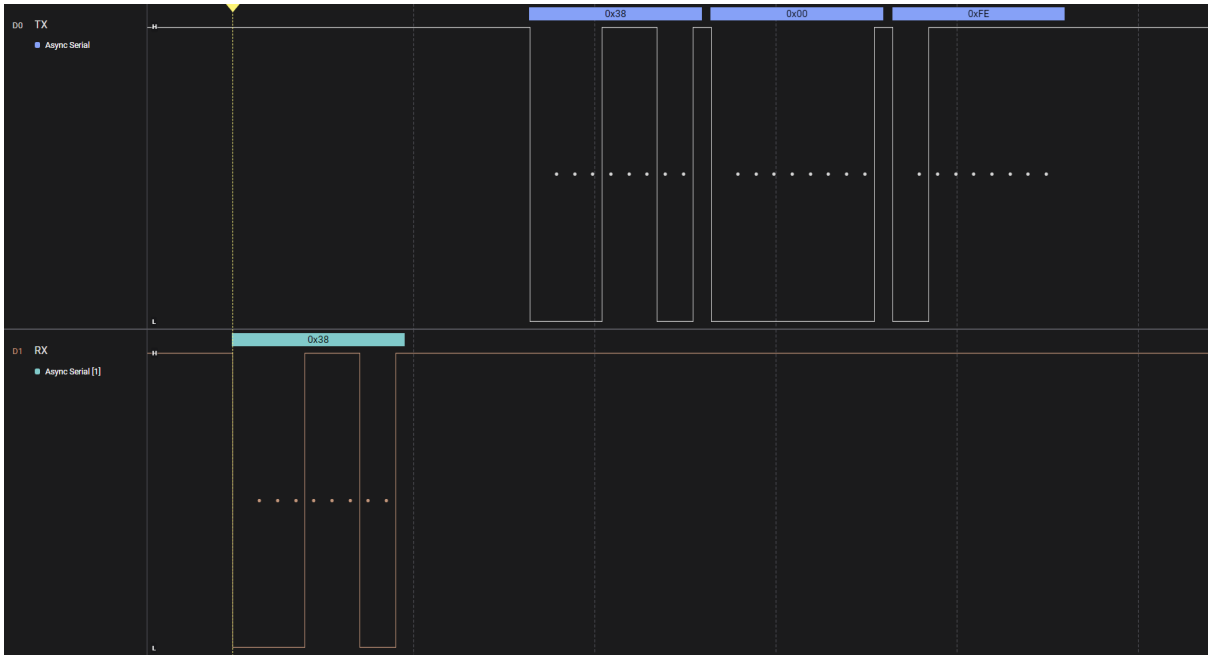

Figure 5.7: Logic analyzer read operation

As seen in Figure 5.6, we write to address 0x1C with a RW bit equal to 1 (0x39) with the data 0x00 and 0xFE. In Figure 5.7 we read from the same address but this time with the RW bit equal to 0, the data returned from the MB is the same as the value written previously, proving that the communication is working as intended.

Due to time constraints, the communication between the MB and the MB hub was not tested. But both the MB and the MB hub has been tested individually, but should work as intended if connected together. The MB was connected using the USB UART to LVDS converter as described above, while the MB hub was connected to a AVR128DA48 development board acting like a MB.

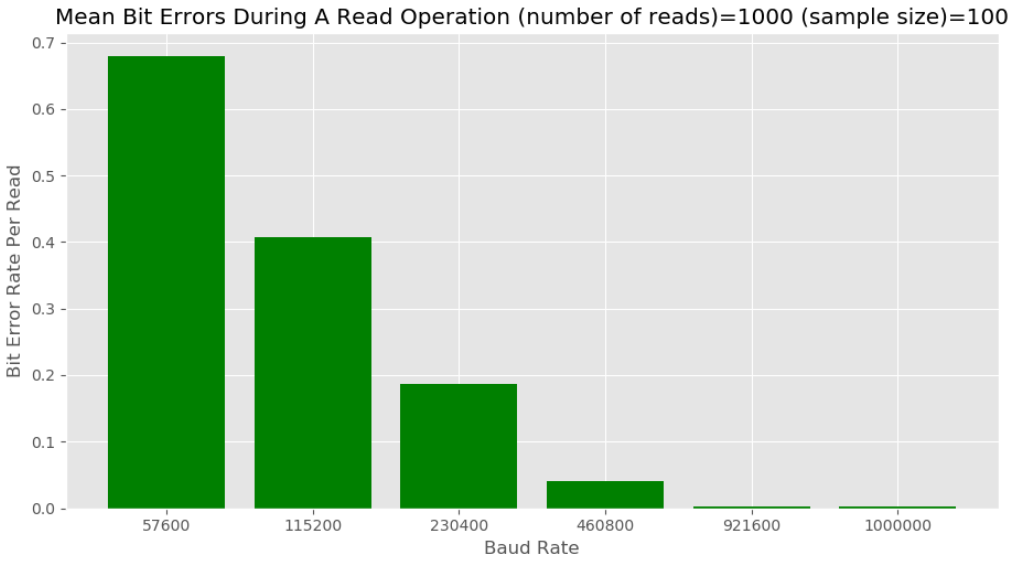

Figure 5.8: Mean bit errors during a read operation of the previous system. Illustration taken from: [5]

The reason for changing from a USART to a UART interface was due to errors in the communication. Both the MB and MB hub was tested using the same stress tests as the previous system. The test writes a random 16-bit value to a given register inside the MB, then reads from the same register 1000 times. This was repeated 100 times at different baudrates to give us a mean number of errors. The results lead to errorless communication, deeming the new UART implementation a success.

5.5 Backplane

Since the backplane only houses connectors and a few passive components, most of the tests to be done on the backplane are simple electrical tests with a multimeter. Albeit simple, the tests need to be completed to ensure that the board is not a safety risk due to faults such as unwanted shorts. Then follows some fitment tests to see if the board both fits and can be mounted into the subrack.

Test	**Criteria/Expected value**	**Result/Measured value**
Continuity test for the mounting holes and metal plating at the edge of the PCB	All holes and plating are connected to chassis ground	OK

Continuity test between power and ground	No continuity (no ground short). Overload (O.L).	OK
Verification of the power-switch functionality for the "Power L" layer	Pins 1 and 1a on the WAGO-connector for the switch should switch on and off connection from the input WAGO-connector to the plane carrying voltage to pin 13 on the PSUs	Silkscreen is wrong; 1 and 1a need to switch place. Otherwise OK.
Verification of the power-switch functionality for the "Power N" layer	Pins 2 and 2a on the WAGO-connector for the switch should switch on and off connection from the input WAGO-connector to the plane carrying voltage to pin 14 on the PSUs	Silkscreen is wrong; 2 and 2a need to switch place. Otherwise OK.
Resistance measurement between chassis and signal ground planes	$>$ 10 GΩ (O.L) when coupling-resistor **is not** mounted. $\approx$ 1 MΩ when coupling-resistor **is** mounted.	OK
Verify mounting hole spacing	Mounting holes should line up with holes in the mounting bracket in the rack. 20.32 mm distance between each hole	OK
Verify DIN41612-connector distance from board edge	The mounting holes on the first connector should be 7.62 mm from the edge of the board	OK
Verify pitch spacing between DIN41612 connectors	Each pair of PSU and MB should take up 11 HP, equal to 55.88 mm, leaving 1 HP = 5.08 mm between each pair	OK
Verify fitment of components and connectors	Pins and mounting holes align with the board	Mounting holes for the DIN-connector does not align with the holes on the board. Otherwise OK.

Table 5.2: Backplane testplan

5.6 System test

After bench testing both the monitor board and the backplane, a system test is next on the list. Before we could test anything, though, we realized that the DIN-connectors were designed such that when we inserted the monitor board connector into the connector on the backplane, they get connected reversely, like this: 1-15, 2-14 ... 15-1. This means that the connections made in the schematic file are completely reversed. Hence, we can not plug the monitor board directly into the backplane to complete a system test.

To bypass this issue for now and get a system test done with the current PCBs, we have made a makeshift solution with external cables to be able to connect the pins from the PSU to the correct pin on the MB. We have also made the needed corrections for the MB, as detailed in Section 4.1.12. Our intention is to mount everything in the rack, and establish communication with the microcontroller through the MB hub. However, we simply lack the time needed to complete this system test, and have to rely on the bench tests performed earlier in this section.

Figures 5.9, 5.10 and 5.11 show the setup for the system test as it is now. The sidepanels have been taken off to improve accessibility during testing:

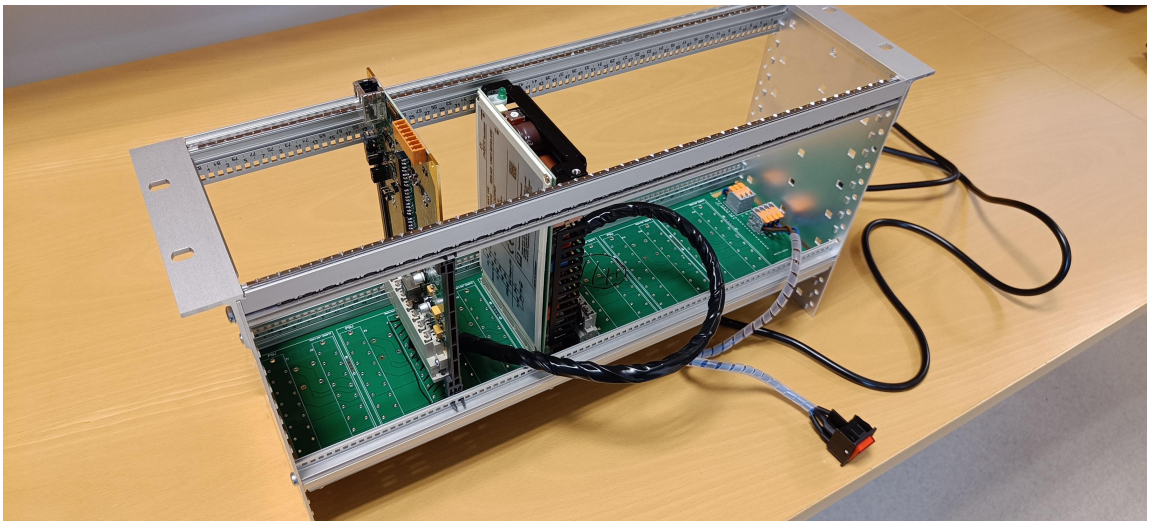

Figure 5.9: Setup for system test - tilted

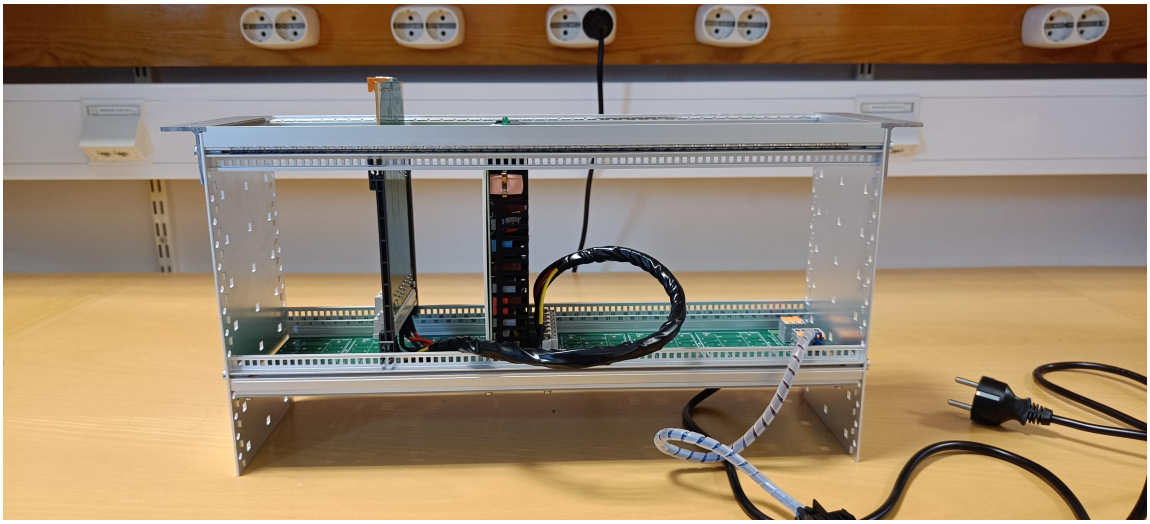

Figure 5.10: Setup for system test - head on

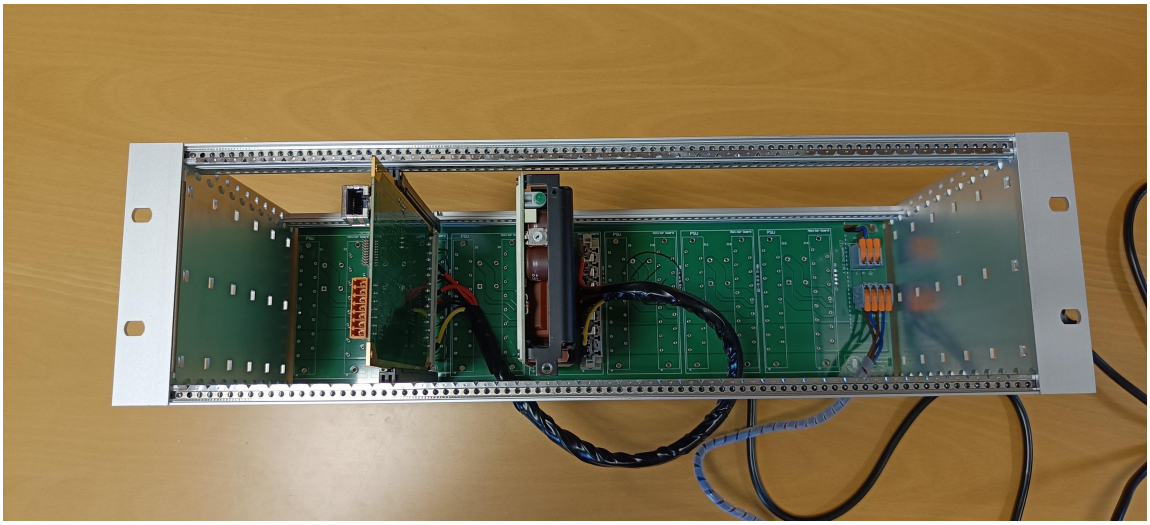

Figure 5.11: Setup for system test - from above

6 Discussion

The first revision of the progress plan, Figure B.1, was a good starting point and outline for the timing of the project, but some deviations were done already week one. First of all, in order to solve the clock skew bug that existed in the inherited design, we quickly realized that we could not just start with making hardware changes to the monitor board and let the software wait: we had to design the software simultaneously with the hardware. Hence, the software design was expedited six weeks from the initial plan.

In the initial plan we had also set up a deadline for ordering the PCBs on the last week before easter. Due to the inductor issue mentioned in Sections 4.1.2 and 4.2.9, this ended up being delayed by two weeks, with the cards being ordered at the start of the second week after easter. This resulted in the testing of the cards being delayed until the final two weeks before the end of the project, which left little time for extensive testing.

The revised progress plan, Figure B.2, shows how the workload actually ended up being distributed.

Many of the risks described in the risk assessment, Table B.1, we're not encounterng. Some of what we did encounter, though, was that the microcontroller that was used in the inherited design, was not available for delivery until months after the project end date. As mentioned in Section 4.1.8, we had to use a different microcontroller from the same family for testing as these were mounted on development boards which were ready for delivery immediately. This ultimately did not steal much time from the project, except for some time spent studying the data sheets for the two microcontrollers to verify that they were in fact interchangeable in the design. The other risk that we did encounter was that an activity took longer than estimated; the already mentioned issue with the inductors in the ripple filter meant that the time lost in (re)designing the monitor board and the backplane caused us to only be able to sketch a solution for the adapter board, as opposed to making a complete design and ordering it along with the other cards.

The current draw of the MB also proved to not be a problem either. The MB draws 213 mA which is negligible compared to the 16 A that the PSU can deliver and the 13.2 A that the TC consumes.

7 Conclusion

This section will look at the results of the project, some weaknesses in the design that were outside the scope of our project to improve, and make some suggestions on work that can be done to further improve the pCT power delivery system.

7.1 Results

This project has seen the design of a new monitor board for filtering, monitoring and controlling the current delivered to sensitive ALPIDE chips. With this there has been made software for the microcontroller on the board, which is the heart of the design. The power that the monitor board monitors is distributed through a custom made backplane, enabling the system to be packed into subracks. A sketch for an adapter board has been made for connection to the monitor board hub, making it possible to connect more than 43 monitor boards into a single hub. The communication protocol between the monitor boards and the MB hub has been changed from an USART protocol to an UART protocol, resolving the clock skew issue. Along with the new UART protocol, an update to the MB hub design has been made.

7.2 Potential design improvements

An issue that has been mentioned many times in this report; the common mode choke for the $DVDD$ line in the ripple filter sits on the backplane. Having a large inductor in a ripple filter for the power delivery to sensitive ALPIDE chips sitting on the backplane while the rest of the filter is on the monitor board is not an ideal design. A proposed solution to this was to instead use ferrite beads, which, for the same current rating as an inductor, packs a much smaller form factor. This was not implemented due to the frequency response of ferrite beads being deemed unfit for the task. Making the drastic change of replacing the inductors with ferrite beads would also mean that a lot more hours would be needed to design and verify the filter.

Currently, the only functionality that turns on and off the power delivery to the ALPIDE chips are the enable signals from the monitor board to the transition card. Optimally, there would be implemented software driven hardware to switch on and off the power output through the orange 7-pin power connector shown on the bottom right of Figure 4.1, which delivers the power to the transition card. This way, there would be a double barrier for errors; both the enable signals *and* the hardware functionality for switching the power to the 7-pin connector would have to be enabled in order to deliver power to the chips.

The supply voltage to the microcontroller is unfiltered (as only the $AVDD$ and $DVDD$ voltages are ripple filtered). This means that in theory the PWELL output from the microcontroller is unfiltered aswell. Seeing as this is a sensitive part of the circuitry, it would be better off filtered, either on the monitor board or on the transition card.

Lastly, many electrical outlet manufacturers only rate their european outlets for a 10 A continuous current draw. A single power cable supplying seven power supplies the maximum current draw of $7 \cdot 1.6\,\mathrm{A} = 11.2\,\mathrm{A}$ continuously means that the racks may have to

be terminated directly into a fuse box.

7.3 Further work

The adapter board is still just a draft, and a full-fledged design is needed before the complete pCT power system can be assembled and controlled through the FPGA.

Improving on the weaknesses detailed in the previous section would yield a more robust design. Some of the points may be easily solved, such as filtering the PWELL voltage, which can possibly be done with a single RC-filter. Other issues will be more time consuming to fix, such as finding a better solution than the inductor on the backplane, which may require a complete redesign of the ripple filter.

7.4 What was achieved

The project achieved many of its objectives and goals. Even if there were setbacks and issues with the first design, the issues have been accounted for and corrected in the new revisions, and the project has been a success. The new monitor board design is a much more robust design, and the new communication protocol between the monitor boards and the MB hub has been verified to work. The new design is also more modular, making it easier to expand the system.

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Appendices

A Software

A.1 Addressmap

Register name	Address	Number of bits	Unit	Access	Default value	Description
FW_VERSION	0x00	8	-	R	-	Current firmware version.
ADC_VALUE	0x02	12	V/V	R	-	12-bit ADC value.
PT100_READING	0x04	7	°C	R	-	ADC value converted to degrees Celsius.
TEMPERATURE_LIMIT	0x06	7	°C	R/W	-	On measuring a temperature above 'TEMPERATURE_LIMIT' the enable signals will be set low. Error: '0x01'
DAC_VALUE	0x08	10	-	R/W	-	DAC output voltage from MCU. Input from 0x0 to 0x400 creates a output voltage from 0V to 2.048V.
PWELL_VOLTAGE_OUT	0x0A	13	mV	R/W	-	The desired PWELL voltage in millivolt. Writing a value to this register triggers the MCU to create the complementary voltage on the PWELL line.
DVDD_CURRENT_THRESHOLD1	0x0C	13	mA	R/W	-	INA3221 DVDD critical threshold. If the DVDD line exceed this current draw the enable signals are set low. Error: '0x02'
DVDD_CURRENT_THRESHOLD2	0x0E	13	mA	R/W	-	INA3221 DVDD warning threshold. Error: '0x03'
DVDD_VOLTAGE	0x10	13	mV	R	-	INA3221 DVDD shunt resistor measured voltage.
DVDD_CURRENT	0x12	13	mA	R	-	INA3221 DVDD shunt resistor measured current.
AVDD_CURRENT_THRESHOLD1	0x14	13	mA	R/W	-	INA3221 AVDD critical threshold. If the AVDD line exceed this current draw the enable signals are set low. Error: '0x04'
AVDD_CURRENT_THRESHOLD2	0x16	13	mA	R/W	-	INA3221 AVDD warning threshold. Error: '0x05'
AVDD_VOLTAGE	0x18	13	mV	R	-	INA3221 AVDD shunt resistor measured voltage.
AVDD_CURRENT	0x1A	13	mA	R	-	INA3221 AVDD shunt resistor measured current.
PWELL_CURRENT_THRESHOLD1	0x1C	13	mA	R/W	-	INA3221 PWELL critical threshold. If the PWELL line exceed this current draw the enable signals are set low. Error: '0x06'
PWELL_CURRENT_THRESHOLD2	0x1E	13	mA	R/W	-	INA3221 PWELL warning threshold. Error: '0x07'
PWELL_VOLTAGE	0x20	13	mV	R	-	INA3221 PWELL shunt resistor measured voltage.
PWELL_CURRENT	0x22	13	mA	R	-	INA3221 PWELL shunt resistor measured current.

ENABLE_SIGNALS	0x24	12	-	R/W	-	Writing a '1' to a bit will set the corresponding enable signal high. Writing a '0' will set the enable signal low. String 0 is tied to LSB.
STRING_DVDD_CURRENT_VALUE[n]	0x26+[2n]	13·12	mA	R	-	The DVDD current values for each string after the scan flag has been asserted. In total 12 registers with 13 bits each. Each string register takes two bytes, and the address for the string n is offset by 2n bytes.
STRING_AVDD_CURRENT_VALUE[n]	0x3E+[2n]	13·12	mA	R	-	The AVDD current values for each string after the scan flag has been asserted. In total 12 registers with 13 bits each. Each string register takes two bytes, and the address for the string n is offset by 2n bytes.
STRING_PWELL_CURRENT_VALUE[n]	0x56+[2n]	13·12	mA	R	-	The PWELL current values for each string after the scan flag has been asserted. In total 12 registers with 13 bits each. Each string register takes two bytes, and the address for the string n is offset by 2n bytes.
ENABLE_SCAN_DELAY	0x6E	16	ms	R/W	-	The delay between enabling a string and scanning the current values. This is to allow the current to stabilize before reading the current values.
RTC_PERIOD	0x70	16	-	R/W	-	The period between each data fetch from the INA3221 and the ADC.
CTRL	0x72	16	-	R/W	-	Control register.
ERROR_COUNT	0x74	4	-	R	-	Amount of errors since last clear. Cleared by writing '1' to control register bit 5.
ERROR_MESSAGE[n]	0x76+[n]	10·8	error	R	-	Error messages stored in sequence, each byte is an error message. The most reccent error is placed in LSB. Cleared by writing '1' to control register bit 5.

Table A.1: Address map

B Project management

B.1 Project organization

The work was mainly separated into three workloads:

1. Designing the new monitor board
2. Writing and testing the software to be used with the monitor board, along with the MB hub design update to fit the new software
3. Designing the backplane
4. Sketching the adapter board

Erlend has been working exclusively on #2, meanwhile Steffen started out working on #2 for a few weeks and has since been working on #1. Martin began working on #1, until about halfway through, when he began working on #3 and #4.

B.2 Initial progress plan

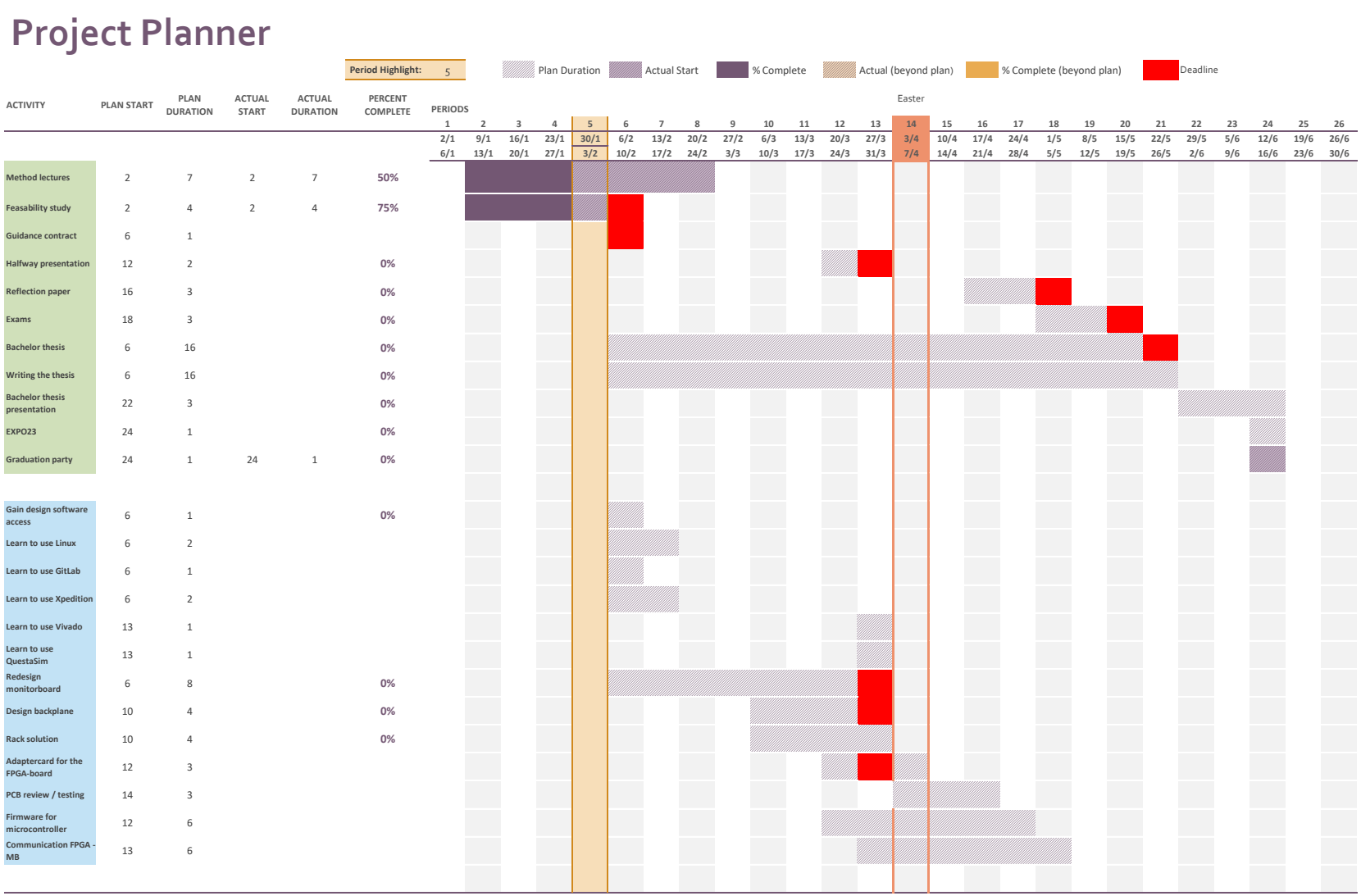


Figure B.1: Initial progress plan

B.3 Revised progress plan

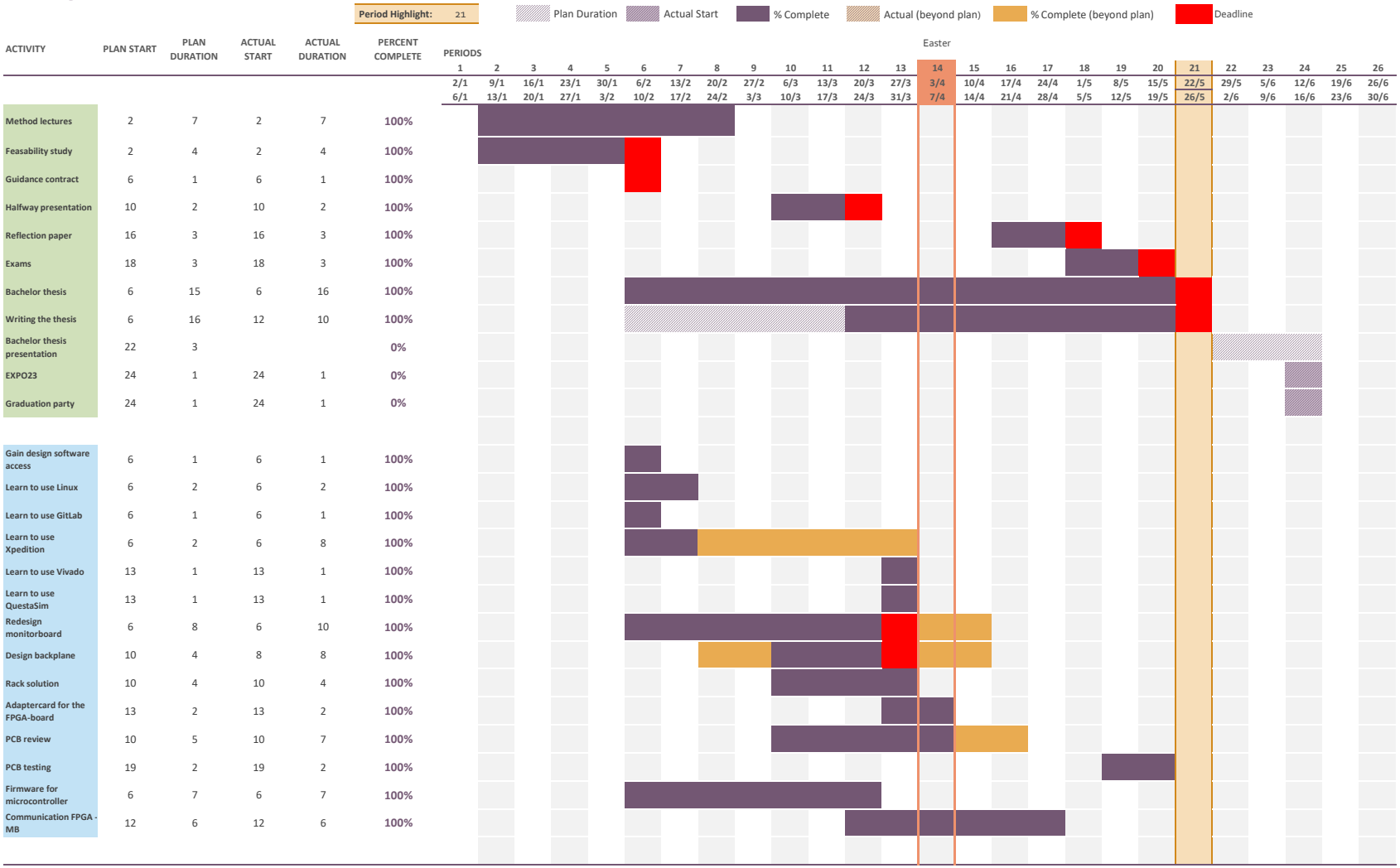


Figure B.2: Revised progress plan

B.4 Risk assessment

Activity	Risk description	Probability (P) (1-5)	Severity (S) (1-5)	Risk value (P x S)	Suggested preventative measures	Actions to be taken upon occurence
General	Project member gets sick	3	2	6	-	Possible to work from home. Other project members carry the workload until the person is back.
Monitor board redesign	Components to be used unavailable to order	2	4	8	Look up component availability when making the PCB design - especially integrated circuits	Look to use a replacement - what does the client (UiB) have in stock etc.
Monitor board redesign	Ordered components not arriving in due time	2	4	8	Order the needed components with a margin for uncertainties in the delivery time	Look to use a replacement - what does the client (UiB) have in stock etc.
All PCB design	PCB not working as intended	2	5	10	Thorough inspection of the design before order	If time (enough weeks left), make the needed changes to the design and reorder. Otherwise, document what has gone wrong and why the error lead to the failure mode.
Software design	Software not working as intended / software bug	4	2	8	Test procedures. Software design thinking before code writing.	Rewrite software to remove bug/fault, log the bug to keep track. Not as time-critical as hardware issues, and faster to resort.
Project management	An activity in the project plan takes more time/work than initially estimated	3	3	9	Help from client (UiB) supervisor to make good estimated on time needed for each activity.	Aquire time from other activities in which we are positive we can complete with less than estimated time. Reprioritize which activities need to be completed in accordance with the list of requirements in Section 3.

Table B.1: Risk assessment

C Other diagrams

Use this appendix if it is not natural to have such diagrams as a part of the main document.

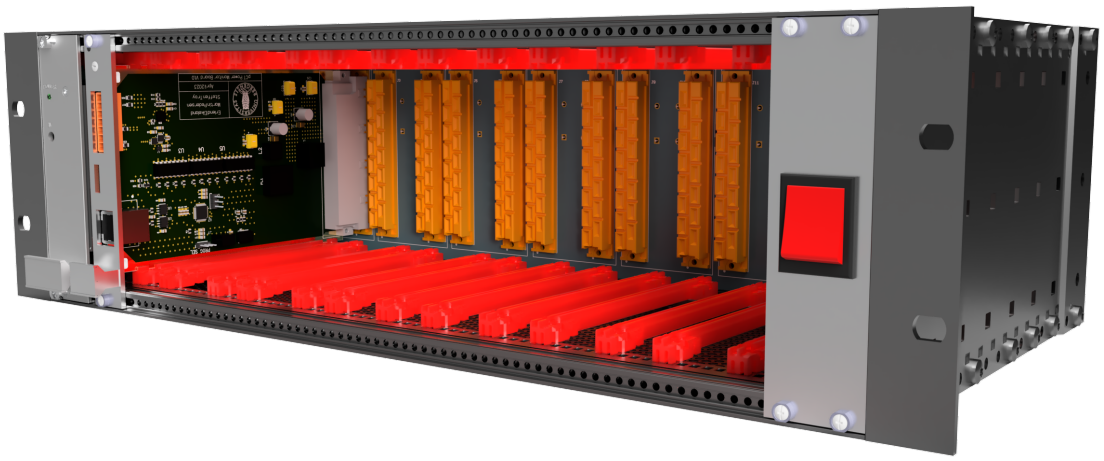


Figure C.1: Subrack tilted

C.1 Power filters

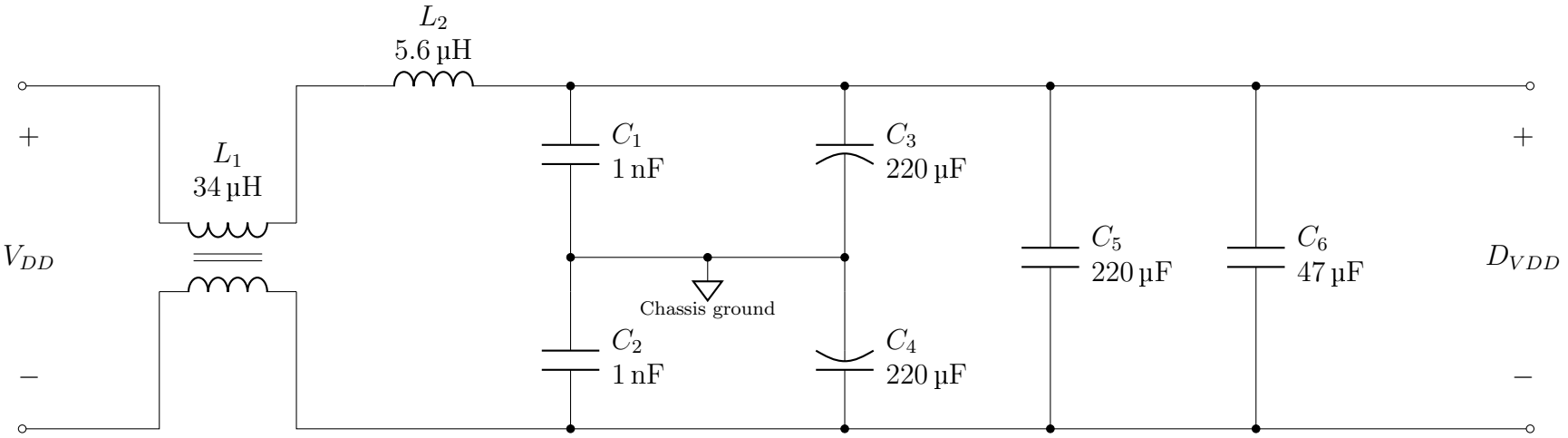


Figure C.2: DVDD filter design

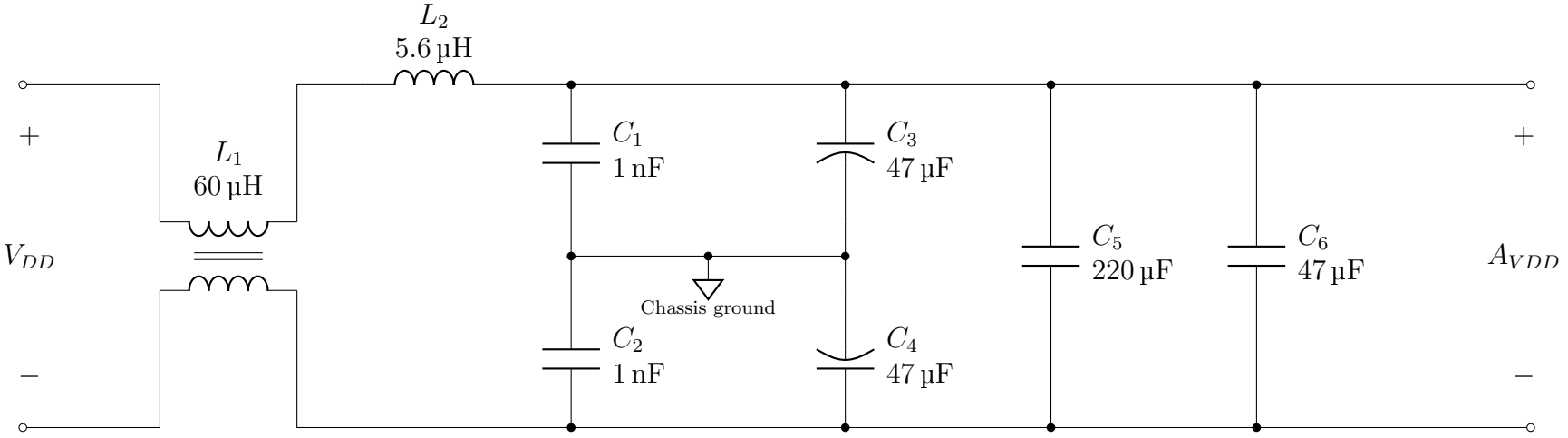
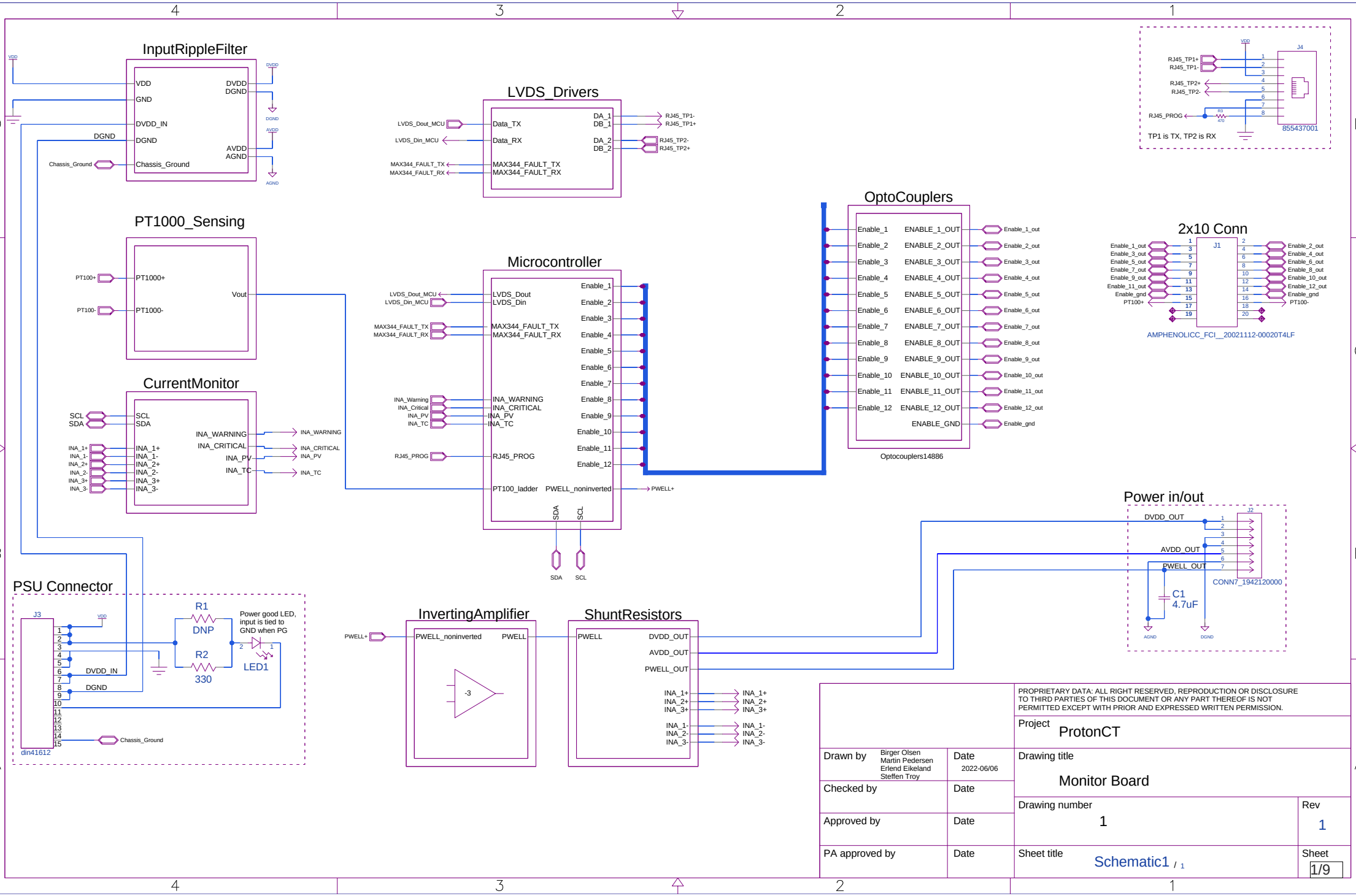


Figure C.3: AVDD filter design

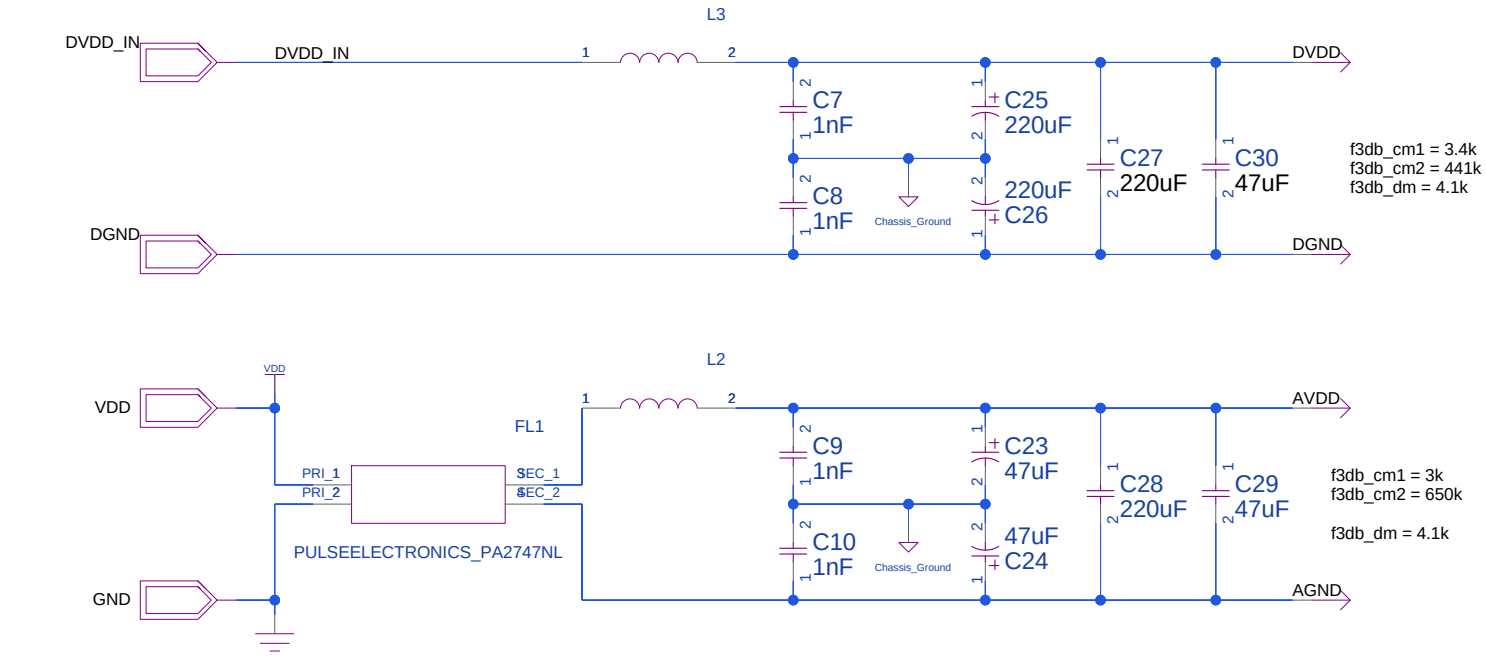
D Design attachments

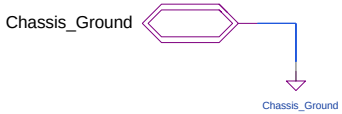
D.1 Schematics

D.1.1 Monitor Board

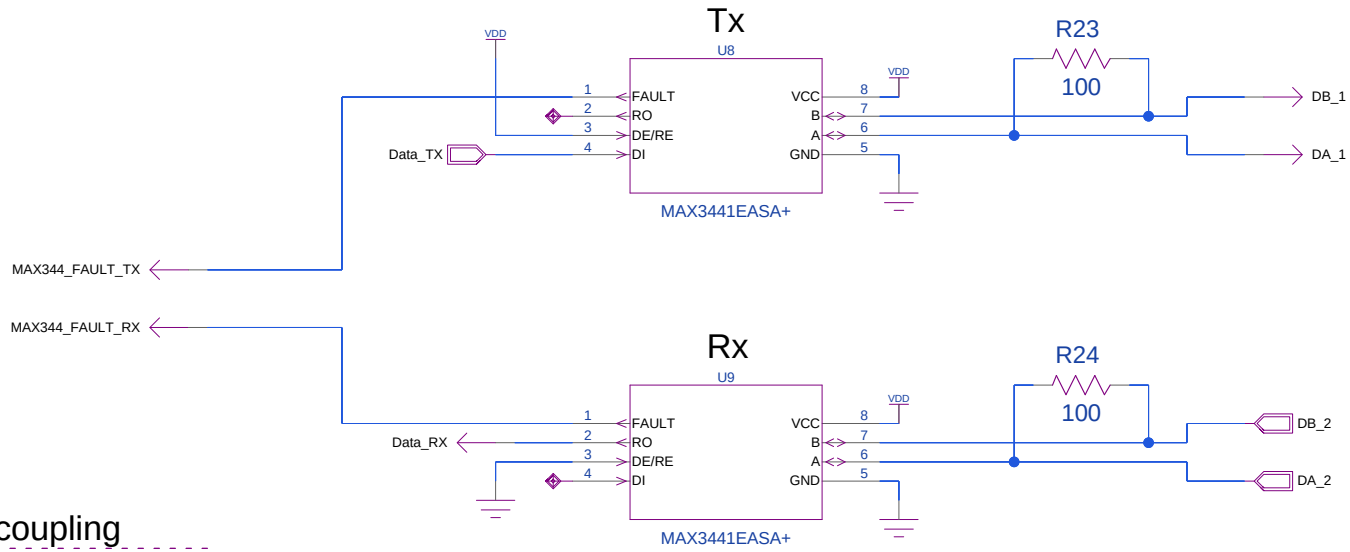


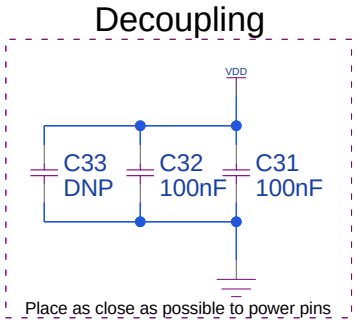
Project	ProtonCT		
Drawn by	Birger Olsen Martin Pedersen Erlend Eikeland Steffen Troy	Date	2022-06/06
Drawing title	Monitor Board		
Checked by		Date	
Drawing number	1	Rev	1
Approved by		Date	
PA approved by		Date	
Sheet title	Schematic1 / 1	Sheet	1/9



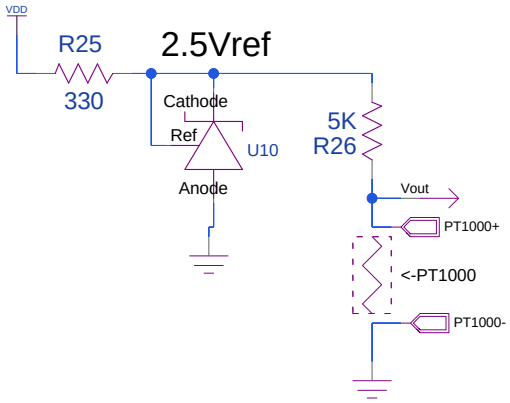


Project: ProtonCT			
Drawn by: Birger Olsen, Martin Pedersen, Erlend Eikeland, Steffen Troy	Date: 2022-06/06	Drawing title: Input ripple filter	
Checked by	Date		
Approved by	Date	Drawing number: 1	Rev: 0
PA approved by	Date	Sheet title: Input_Ripple_Filter / 1	Sheet: 2/9





Project: ProtonCT			
Drawn by: Birger Olsen, Martin Pedersen, Erlend Eikeland, Steffen Troy	Date: 2022-06/06	Drawing title: Differential Signaling Drivers	
Checked by	Date		
Approved by	Date	Drawing number: 1	Rev: 0
PA approved by	Date	Sheet title: LVDS_Drivers / 1	Sheet: 3/9



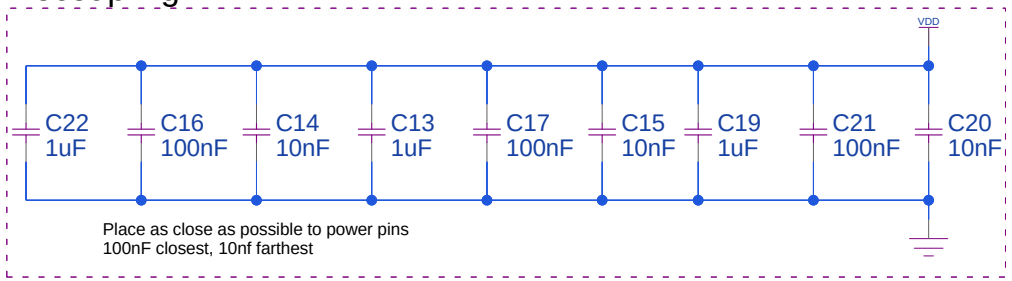
i_min_100deg = 2.5V/(5k+1385) = 0.39 mA
i_max_0deg = 2.5V/6k = 0.4166 mA

Voltage diff(PT1000) from 0 to 100 = 124mV
ADC sensitivity = 0.61mV

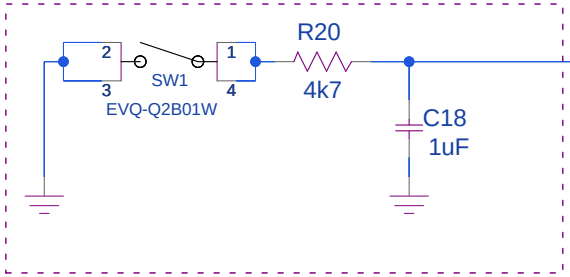
A 0.49 degree change will be noticeable by MCU

Project: ProtonCT			
Drawn by: Birger Olsen, Martin Pedersen, Erlend Eikeland, Steffen Troy	Date: 2022-06/06	Drawing title: Temperature Sensing	
Checked by	Date		
Approved by	Date	Drawing number: 1	Rev: 0
PA approved by	Date	Sheet title: Sensing / 1	Sheet: 4/9

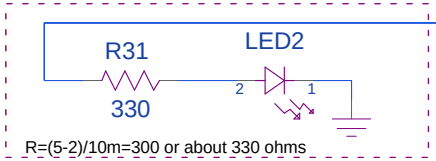
Decoupling



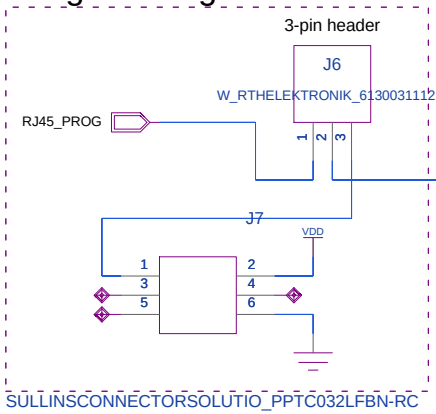
Reset switch



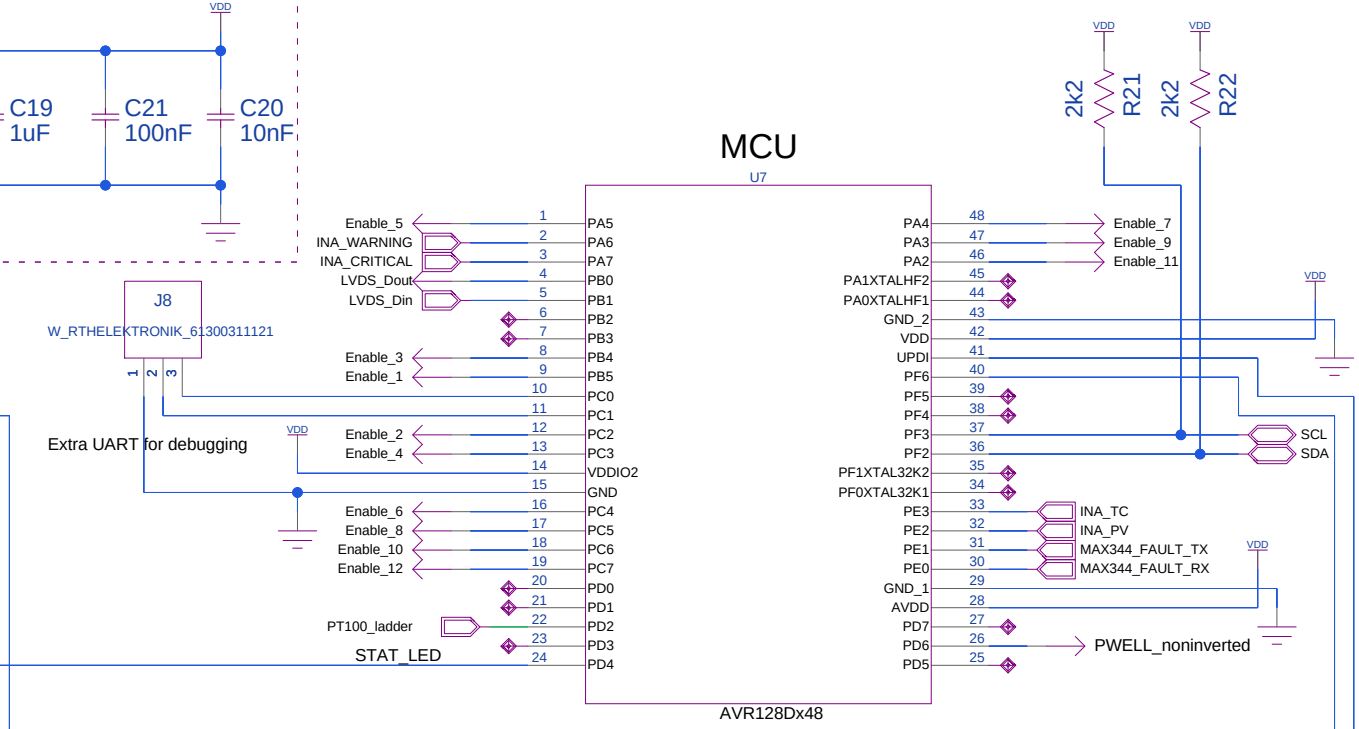
Status LED



Programming

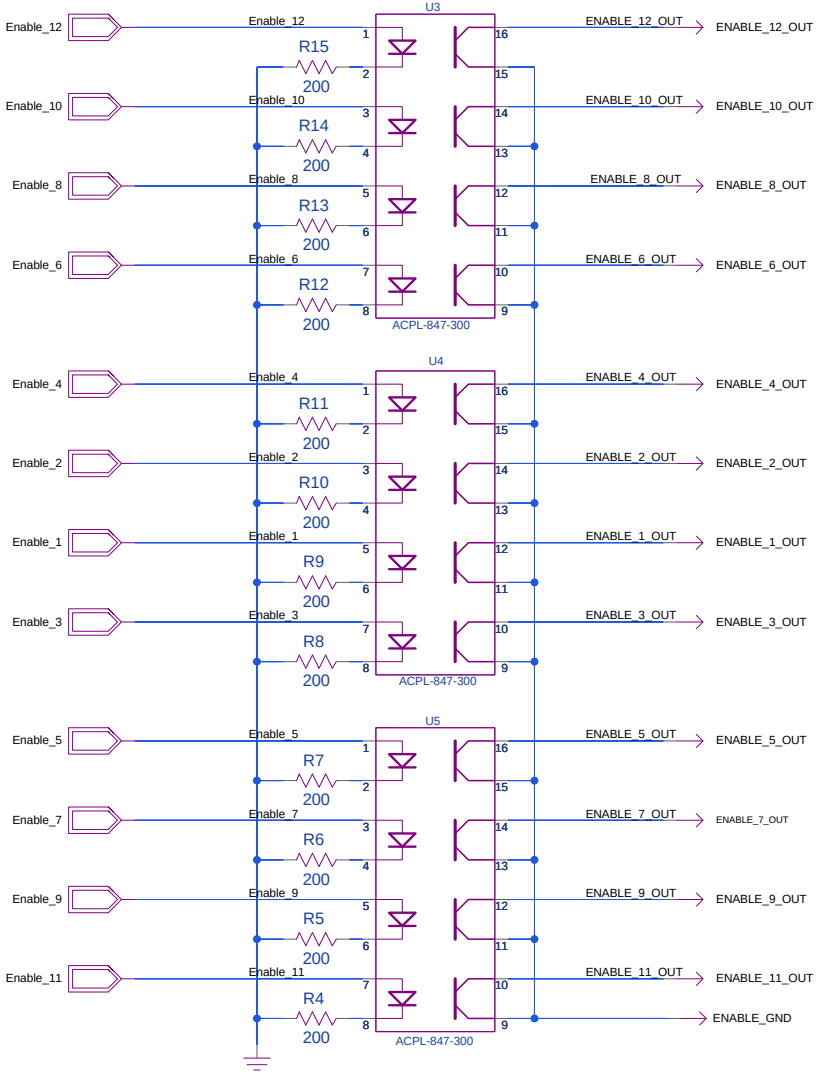


MCU



Project	ProtonCT		
Drawn by	Birger Olsen Martin Pedersen Erlend Eikeland Steffen Troy	Date	2022-06/06
Drawing title	Microcontroller		
Checked by		Date	
Drawing number	1	Rev	0
Approved by		Date	
PA approved by		Date	
Sheet title	Microcontroller / 1	Sheet	5/9

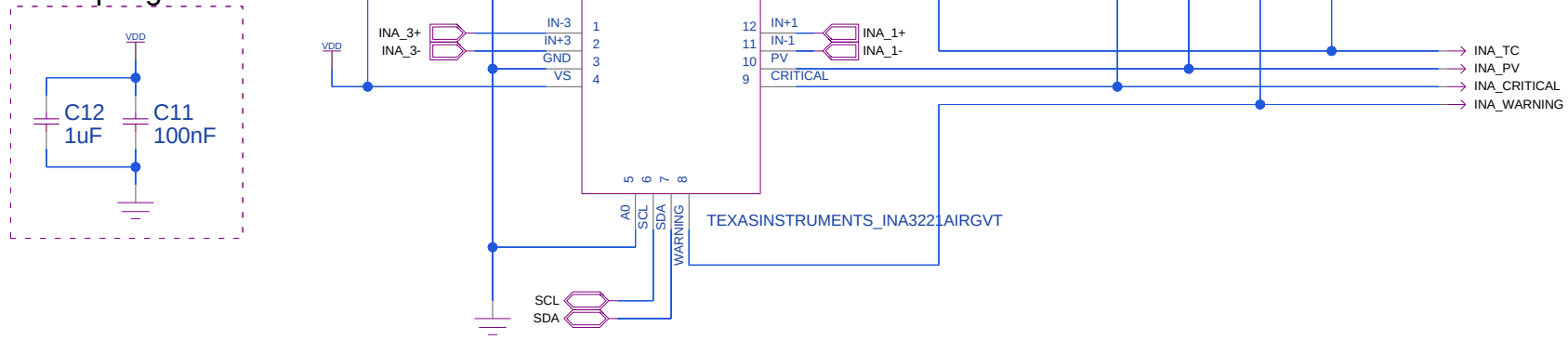
The pin numbers are not random, they have been optimized to account for layout



If = 20mA
Vf = 1.2V

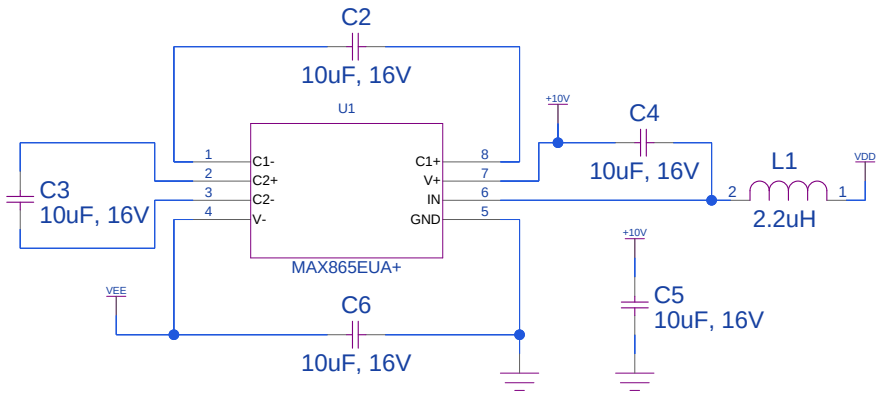
V/R = 3.8/200 = 19mA

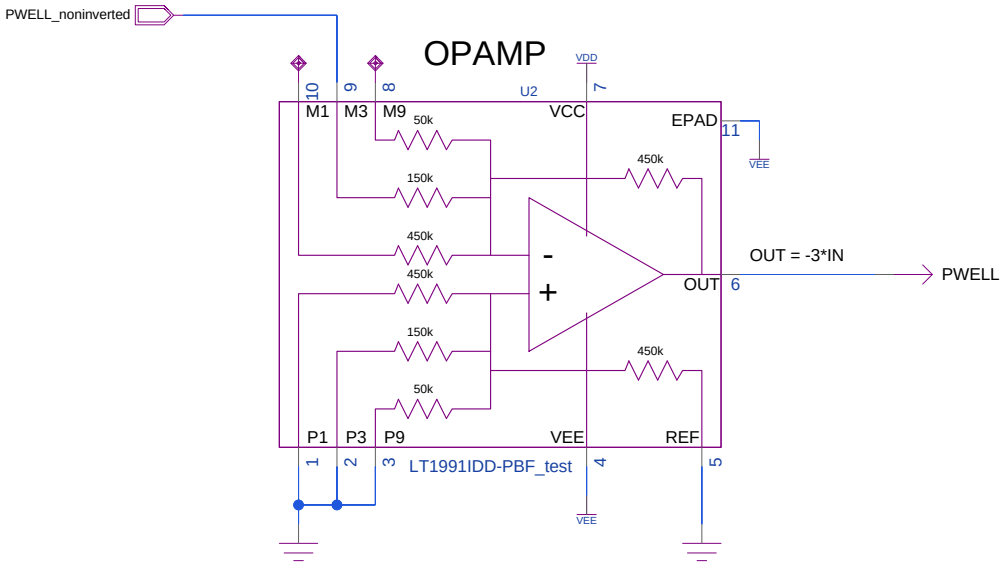
Project	ProtonCT		
Drawn by	Birger Olsen Martin Pedersen Erlend Eikeland Steffen Troy	Date	2022-06/06
Drawing title	Optocouplers		
Checked by		Date	
Drawing number	1	Rev	0
Approved by		Date	
PA approved by		Date	
Sheet title	NAME	Sheet	6/9



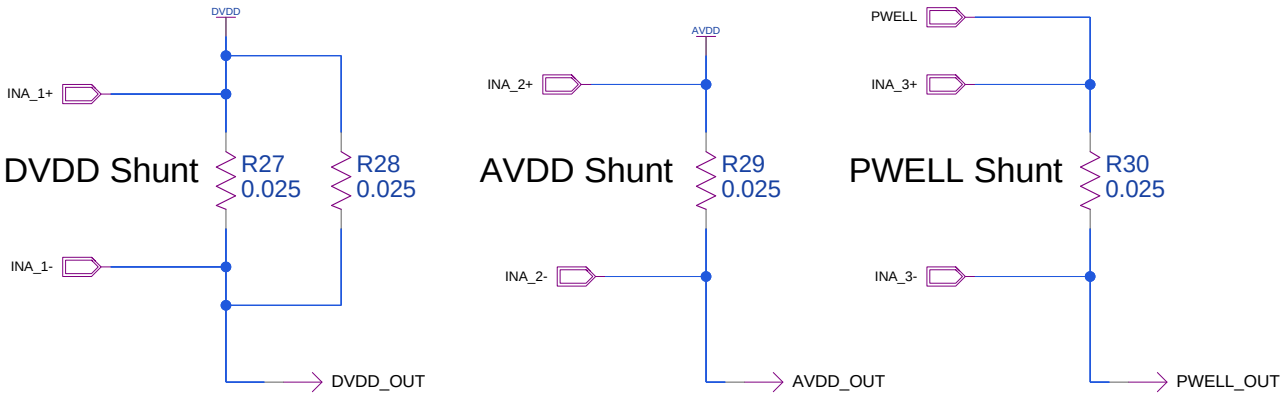
Project: ProtonCT			
Drawn by: Birger Olsen, Martin Pedersen, Erlend Eikeland, Steffen Troy	Date: 2022-06/06	Drawing title: Current Monitor	
Checked by	Date		
Approved by	Date	Drawing number: 1	Rev: 0
PA approved by	Date	Sheet title: CurrentMonitor / 1	Sheet: 7/9

Switched capacitor voltage doubler





Project: ProtonCT		
Drawn by: Birger Olsen, Martin Pedersen, Erlend Eikeland, Steffen Troy	Date: 2022-06/06	Drawing title: Inverting Amplifier
Checked by	Date	Drawing number: 1 / Rev: 0
Approved by	Date	
PA approved by	Date	Sheet title: NAME / / Sheet: 8/9



Project	ProtonCT		
Drawn by	Birger Olsen Martin Pedersen Erlend Eikeland Steffen Troy	Date	2022-06/06
Drawing title	Shunt Resistors		
Checked by		Date	
Drawing number	1	Rev	0
Approved by		Date	
PA approved by		Date	
Sheet title	ShuntResistors / 1	Sheet	9/9

D.1.2 Backplane

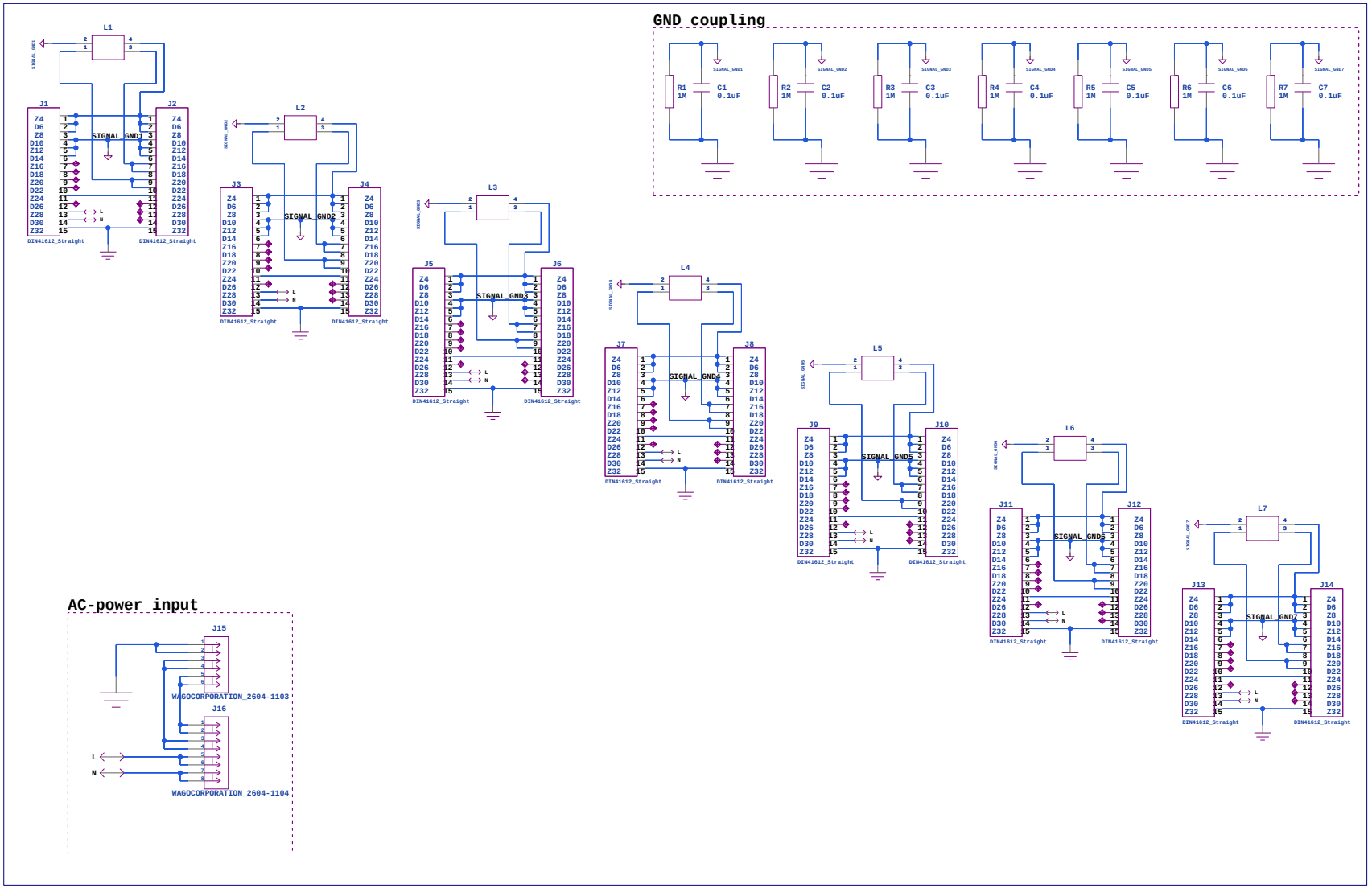


Figure D.1: Backplane schematic

D.2 Layout

D.2.1 Monitor Board

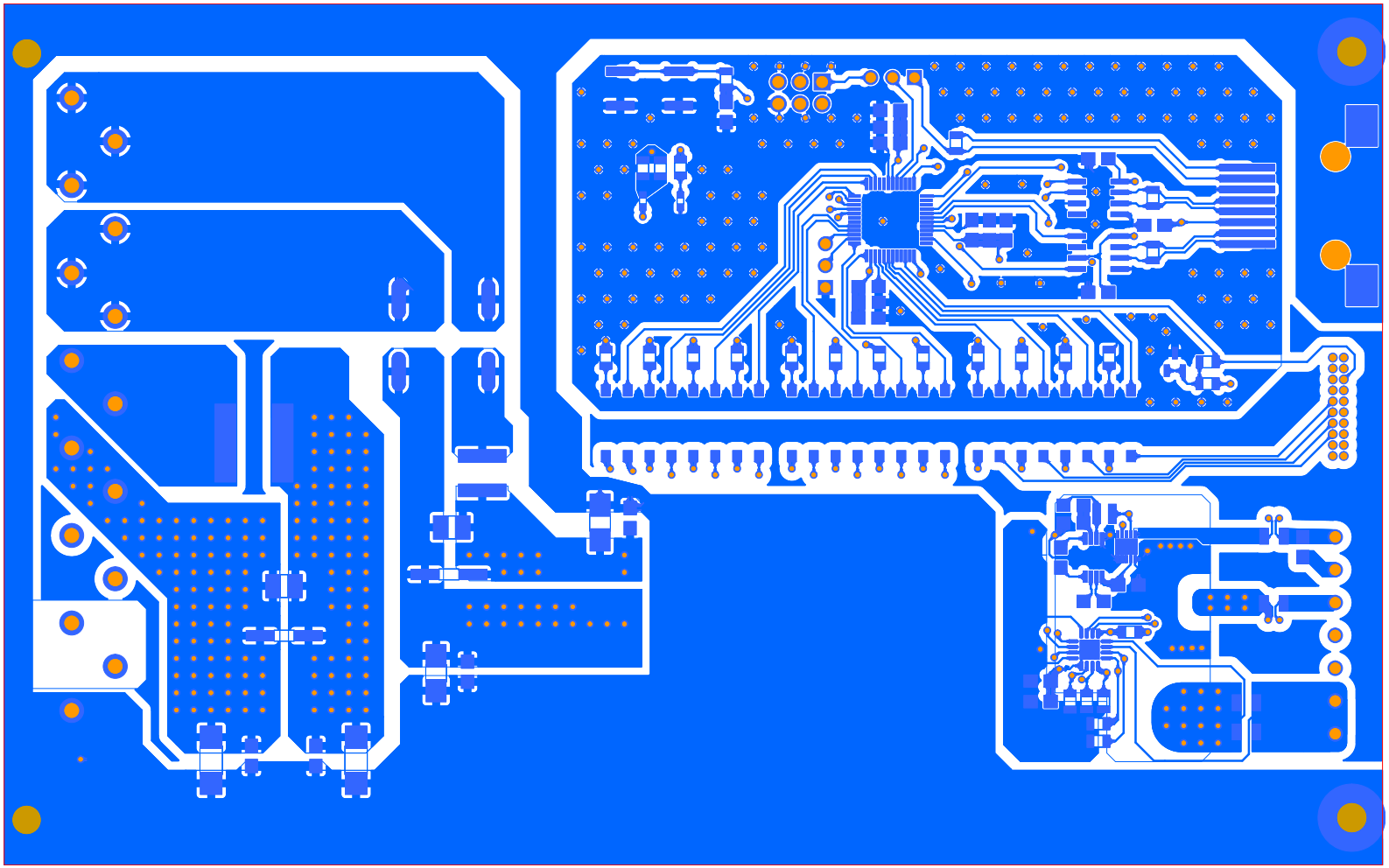


Figure D.2: Monitor Board layer 1 - Signal 1

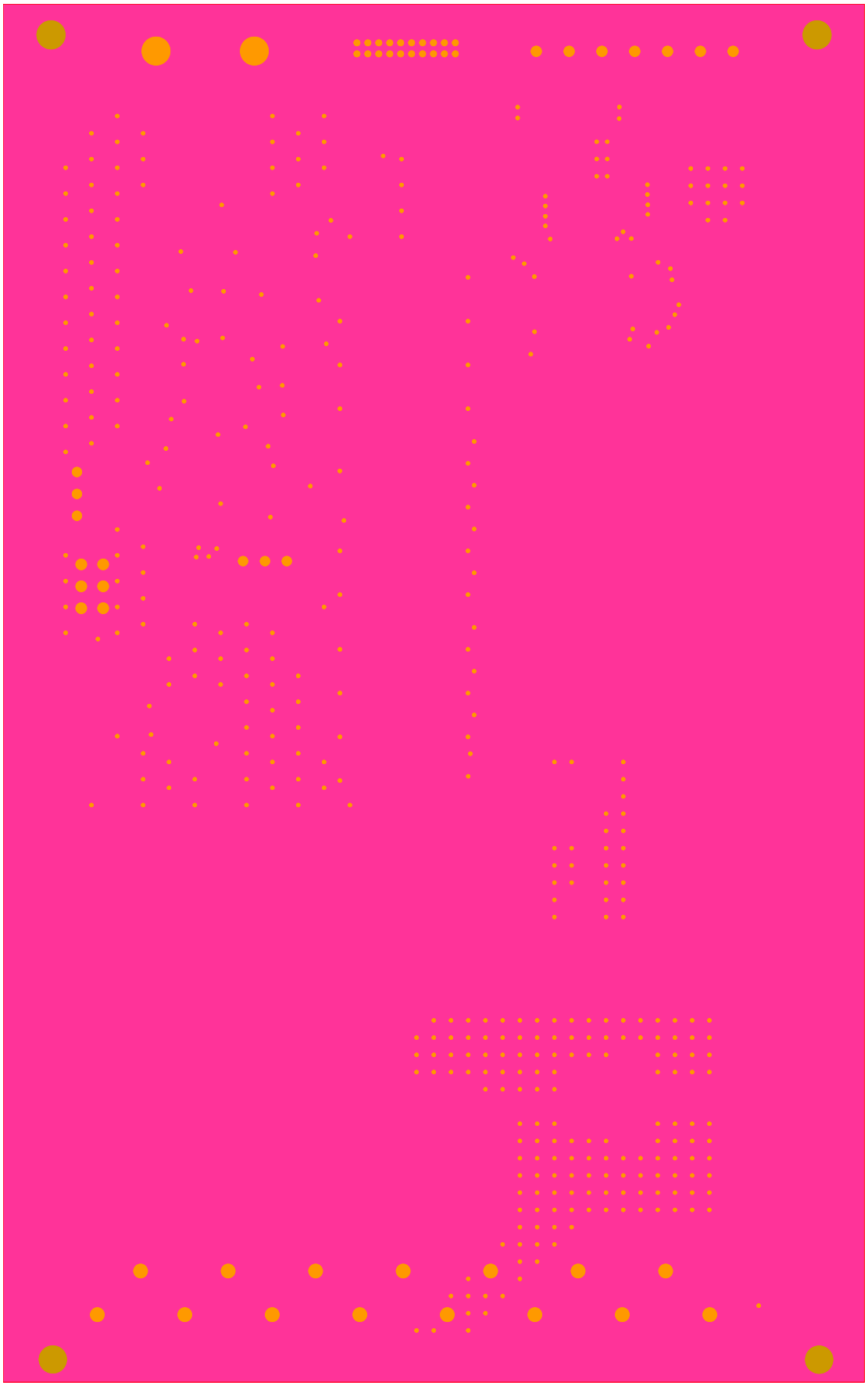


Figure D.3: Monitor Board layer 2 - Shield 1

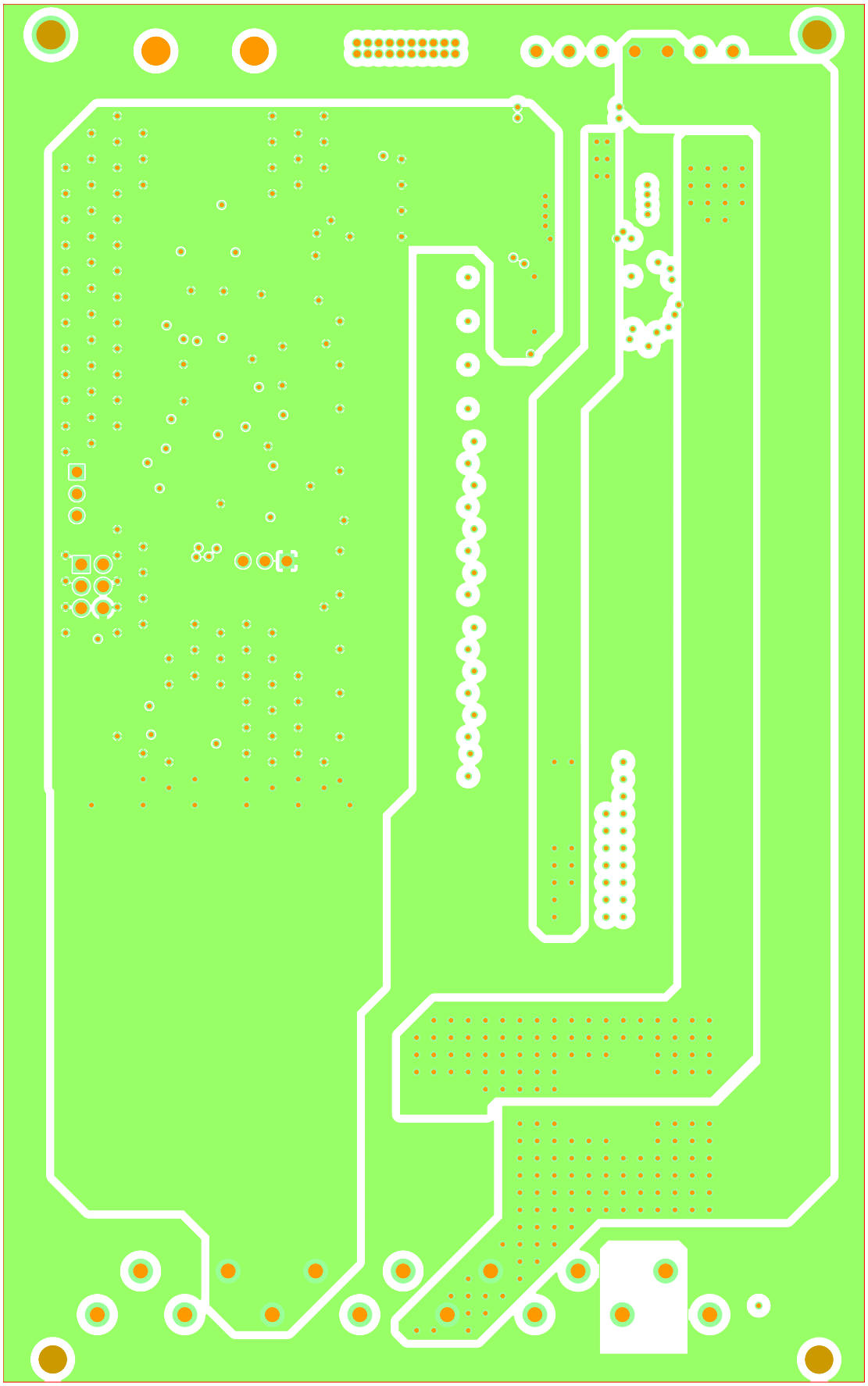


Figure D.4: Monitor Board layer 3 - DGND

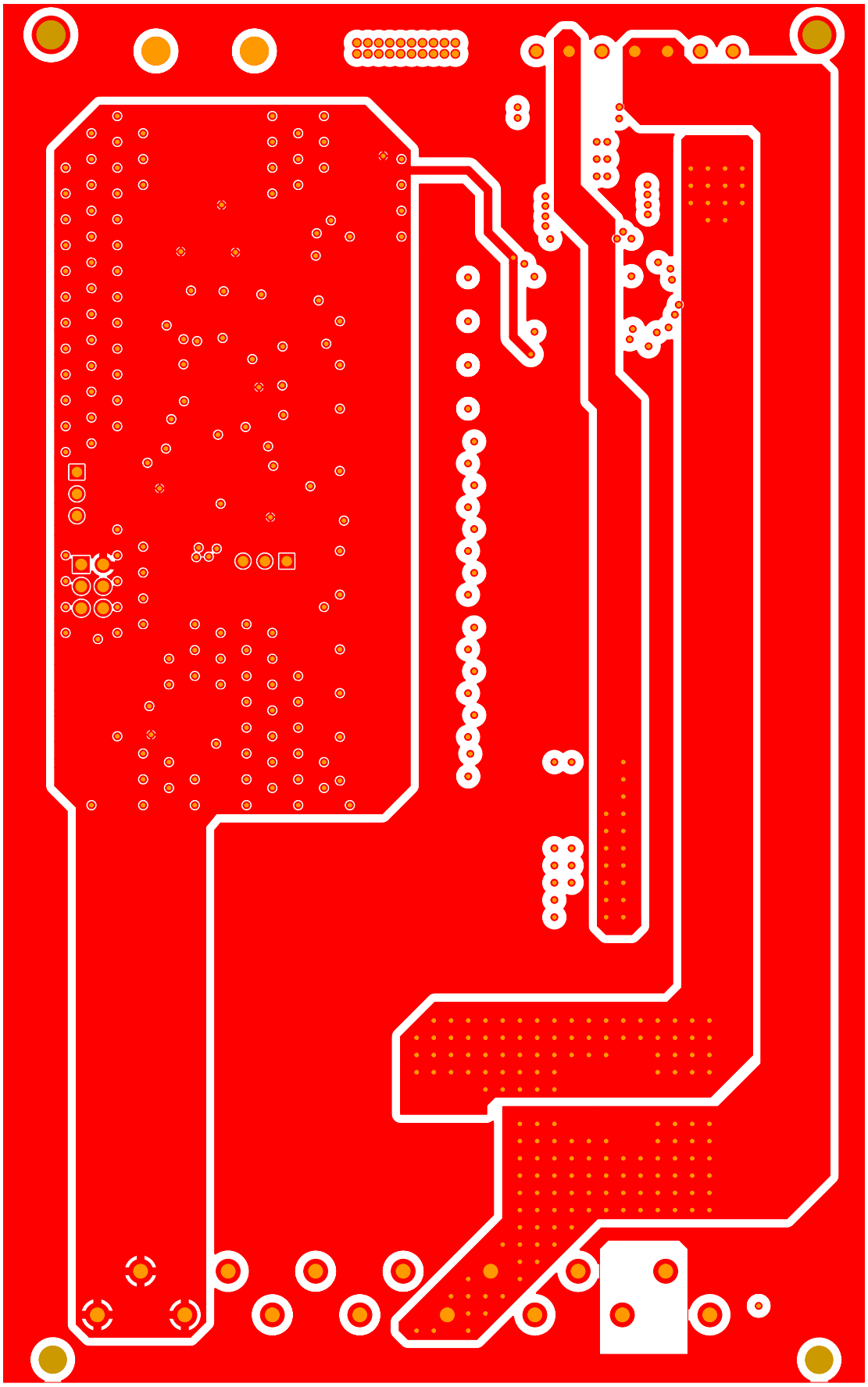


Figure D.5: Monitor Board layer 4 - VDD

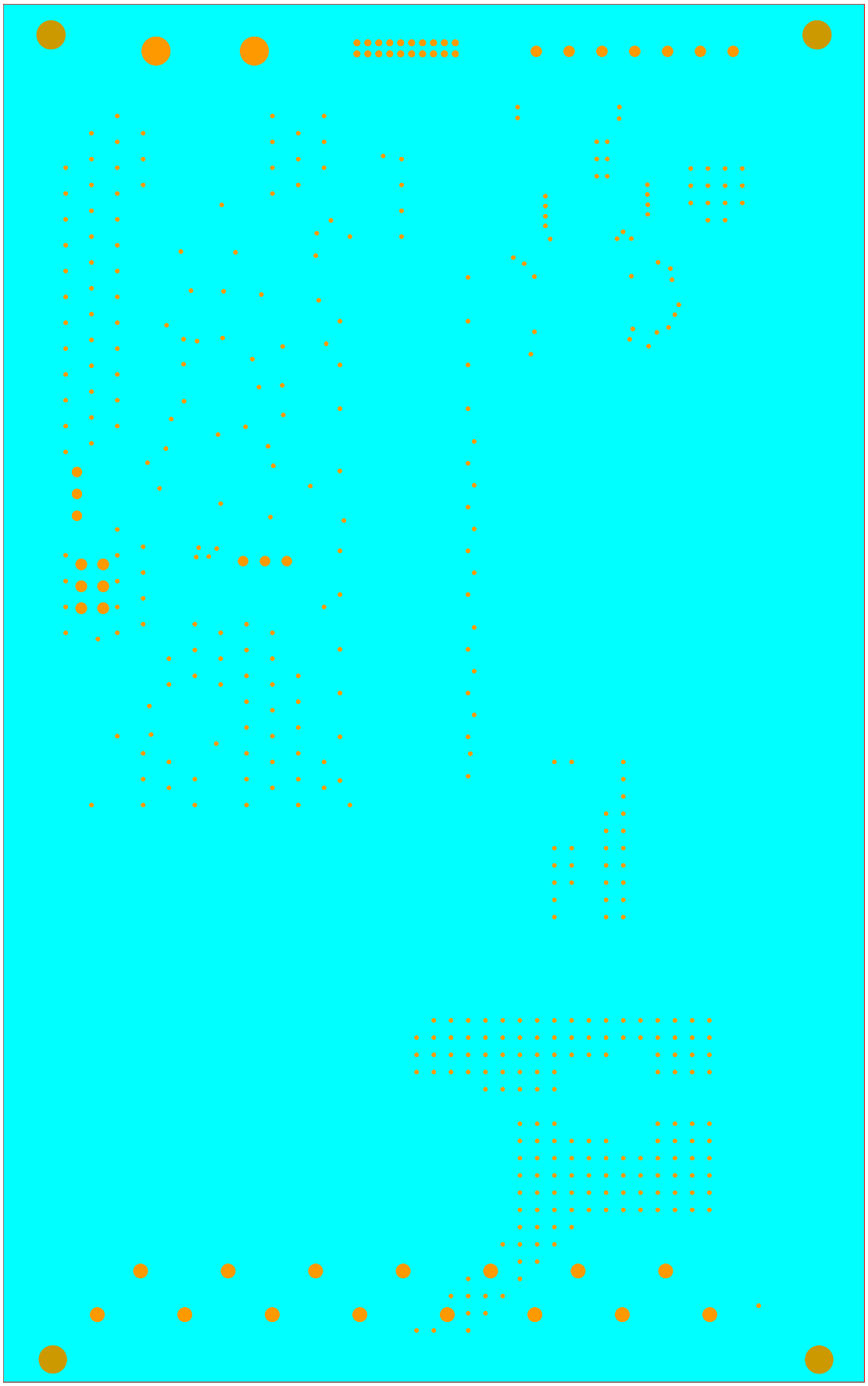


Figure D.6: Monitor Board layer 5 - Shield 2

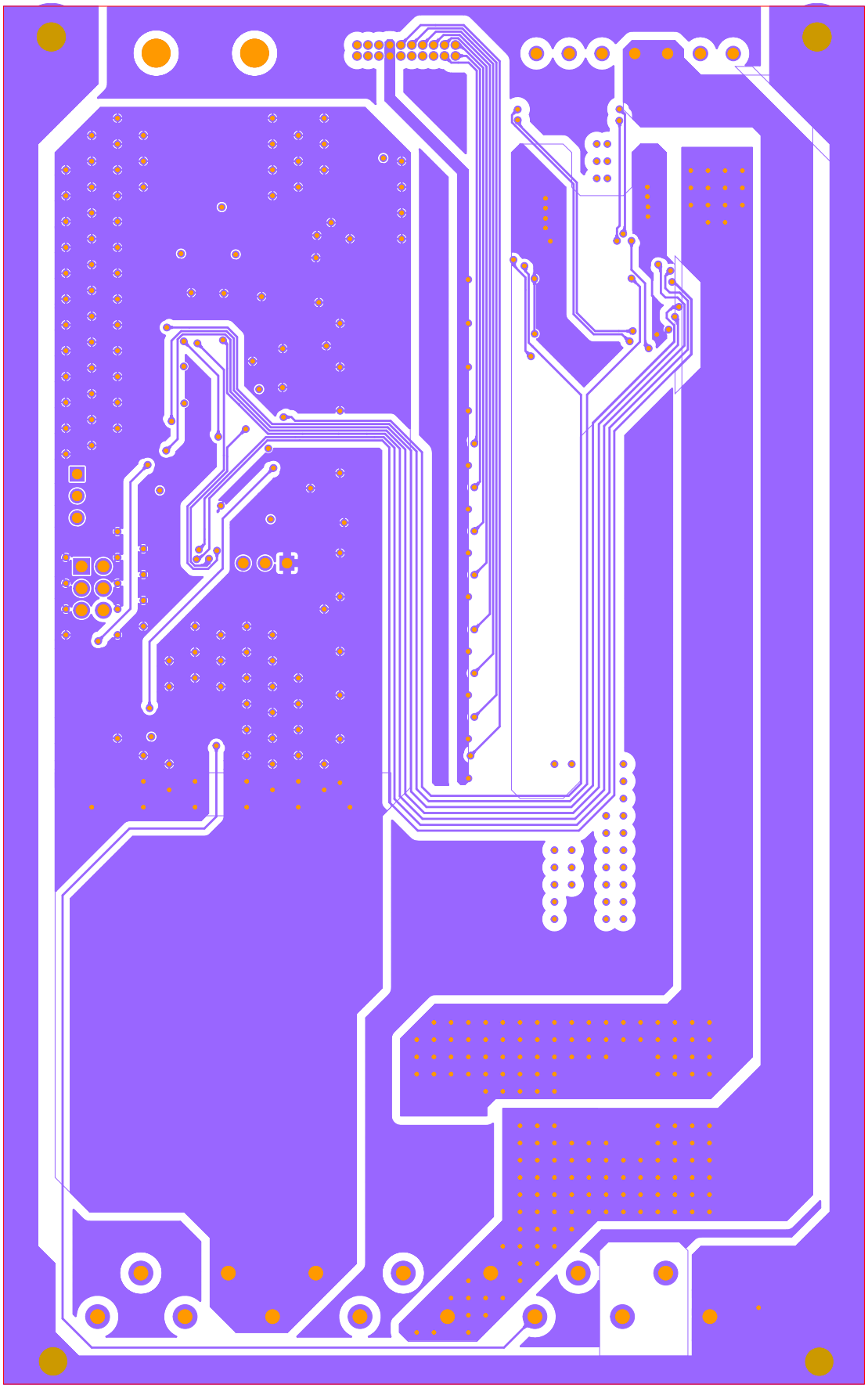


Figure D.7: Monitor Board layer 6 - Signal 2

D.2.2 Backplane

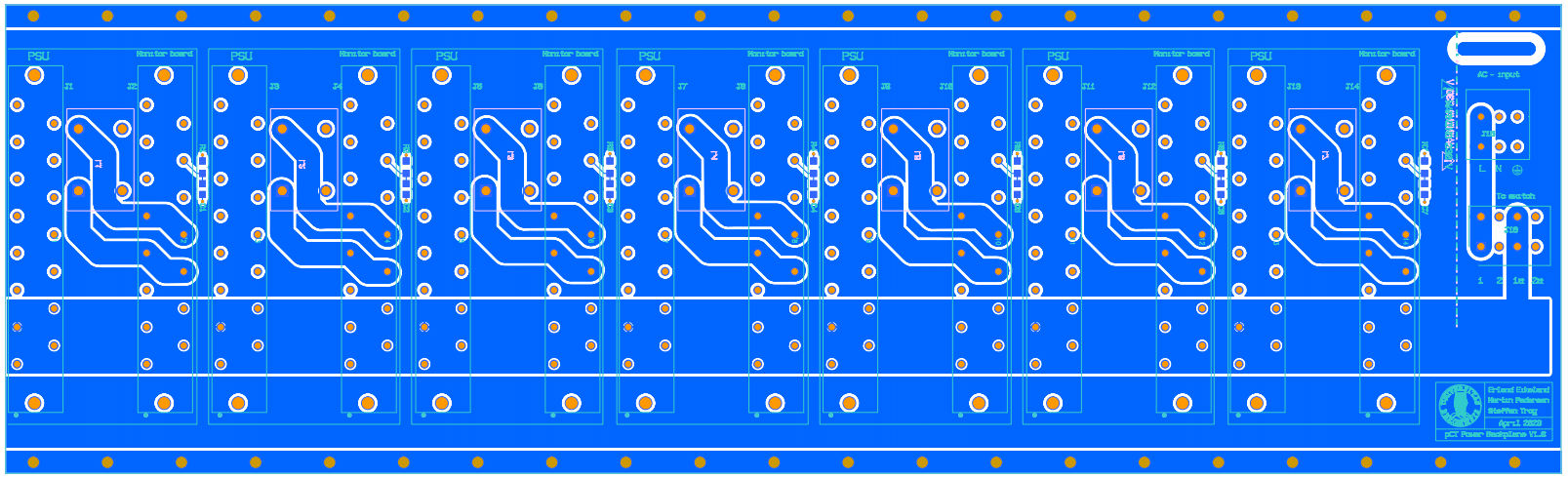


Figure D.8: Backplane layer 1 - AC-L and VDD

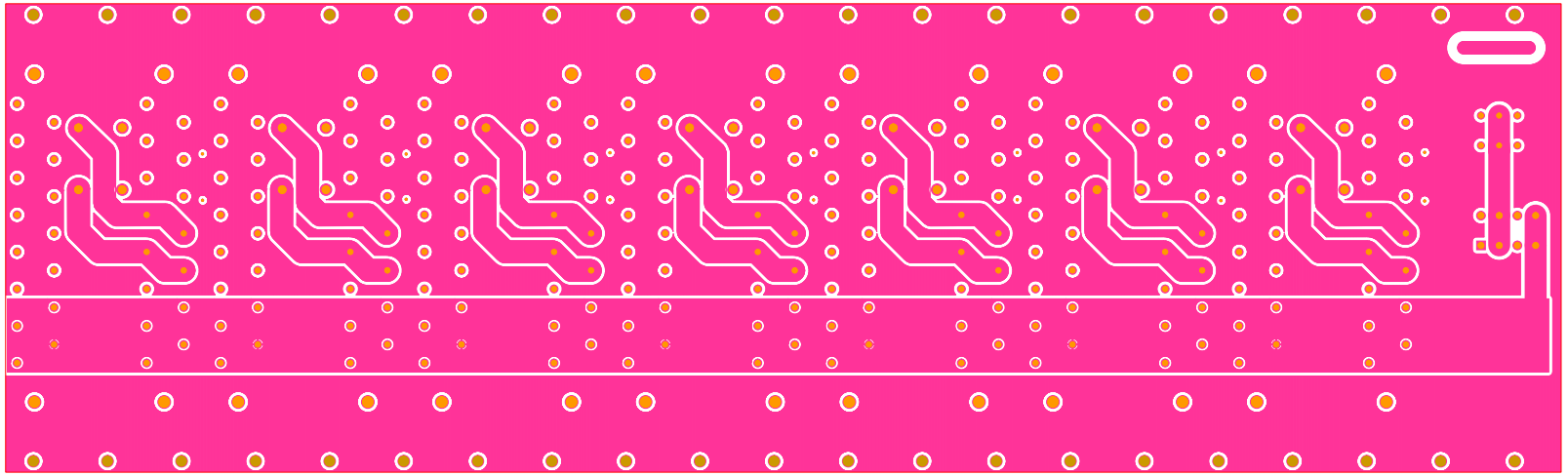


Figure D.9: Backplane layer 2 - AC-N and VDD

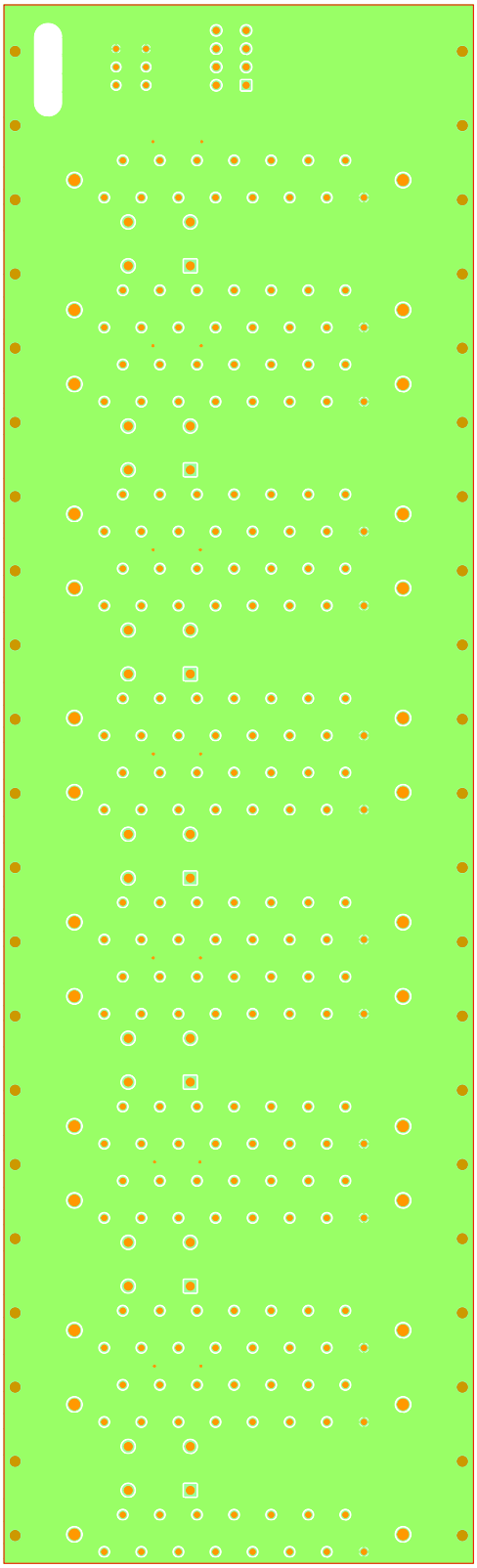


Figure D.10: Backplane layer 3 - Chassis ground

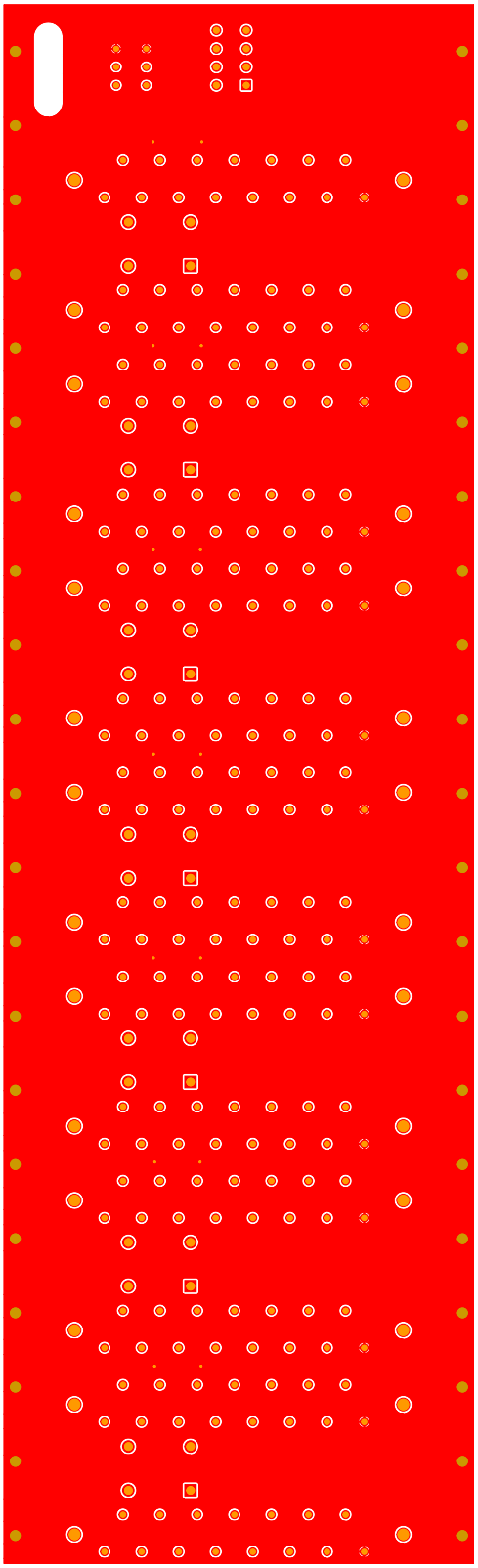


Figure D.11: Backplane layer 4 - Chassis ground

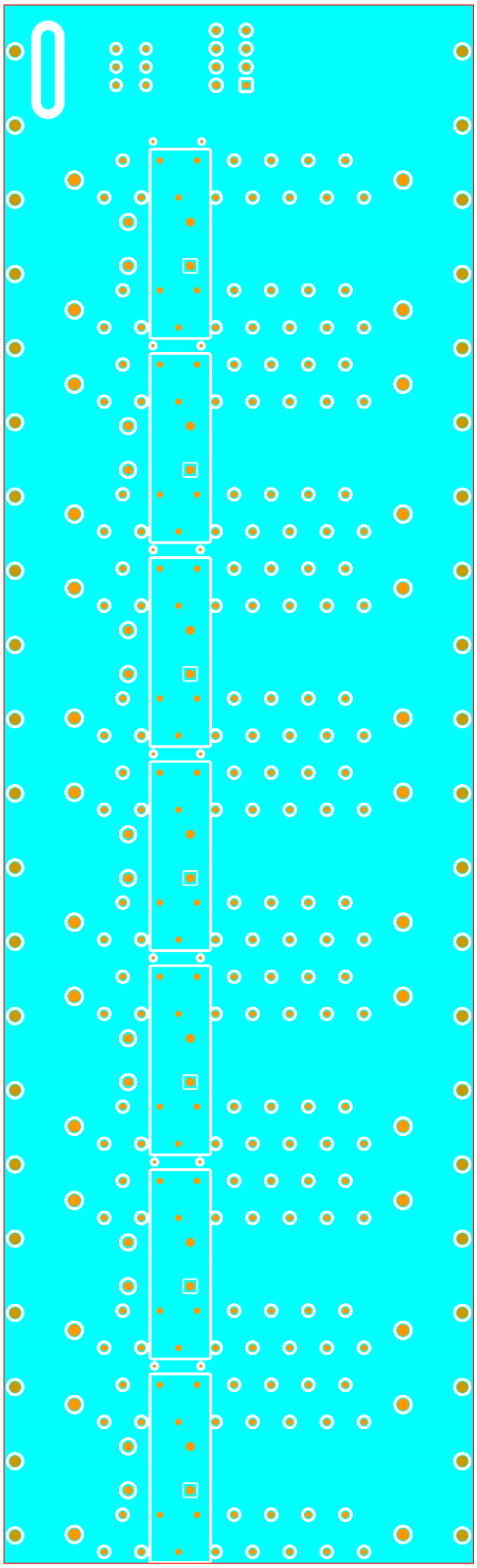


Figure D.12: Backplane layer 5 - Signal ground

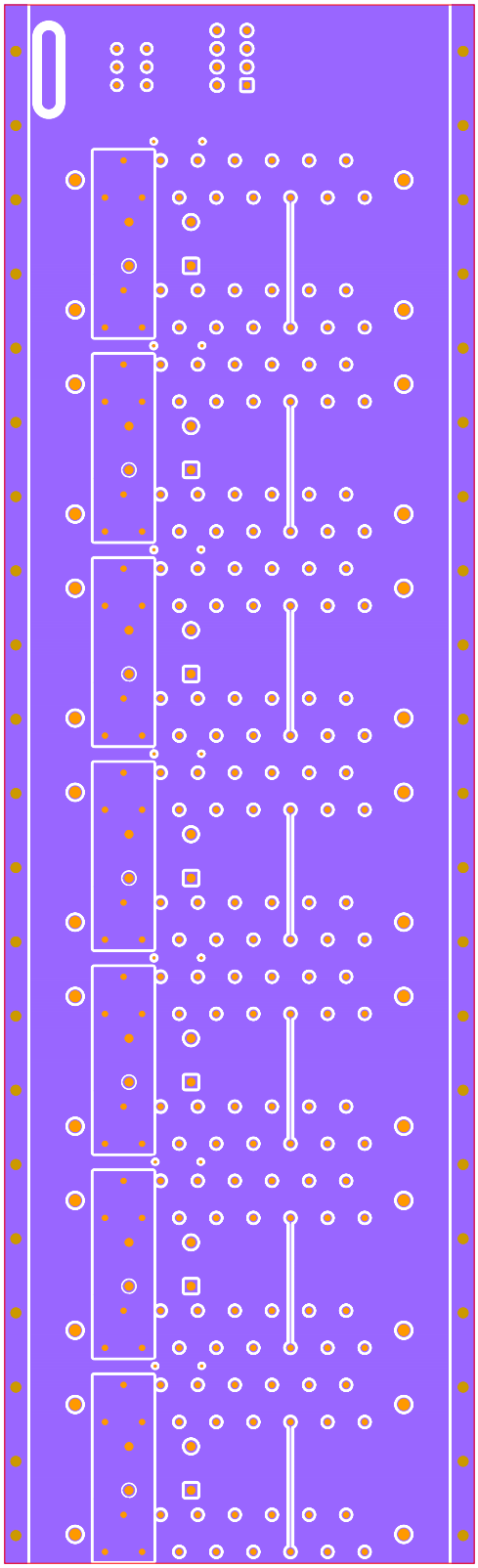


Figure D.13: Backplane layer 6 - VDD

D.3 Bill of Materials

#	Qty	Ref Des	Manufacturer	Mfg Num	Description	Pkg
1	6	C11 C16 C17 C21 C31 C32	KEMET	C0805C104K9RAC7800	$100nF$ $6.3V$	0805
2	3	C14 C15 C20	Würth Elektronik	885012207011	$10nF$ $10V$	0805
3	5	C2 C3 C4 C5 C6	KEMET	C0805C106K4PAC7210	$10\mu F$ $16V$	0805
4	4	C7 C8 C9 C10			$1nF$	0805
5	5	C12 C13 C18 C19 C22	KEMET	C0805C105K4PAC7800	$1\mu F$ $16V$	0805
6	1	C1	KEMET	C0805C475K8PAC7800	$4.7\mu F$ $10V$	0805
7	1	C33	N/A	N/A	DNP	0805
8	4	C23 C24	KEMET	T491C476K016AT	$47\mu F$ $16V$	2312
9	4	C25 C26	KEMET	T495X227K016ATE100	$220\mu F$ $16V$	2917
10	2	C27 C28	KEMET	EXV227M016A9HAA	$220\mu F$ $16V$	
11	2	C29 C30	Murata Electronics	GRM32EC81C476KE15L	$47\mu F$ $16V$	1210
12	1	IC6	Texas Instruments	INA3221AIRGVT	INA3221 Current Monitor	16-VQFN
13	1	J1	Amphenol	2002111200020T4LF	2x10 0.1” pin header	
14	1	J2	Weidmuller	1942120000	7 pin power connector	
15	1	J3	HARTING	09061152932	DIN-41612 H15	
16	1	J4	Molex	855437001	Modular jack 8p8c	
17	2	J6 J8	Würth Elektronik	61300311121	3 pin header	
18	1	J7	Sullins Conn. Solutions	PPPC032LFBN-RC	2x3 0.1” pin header	
19	1	L1	Würth Elektronik	74438323022	$2.2\mu H$ $1.3A$	
20	1	L2	Würth Elektronik	78439346056	$5.6\mu H$ $5.6A$	
21	1	L3	Coilcraft	XAL1010562MED	$5.6\mu H$ $15.7A$	
22	1	FL1	Pulse Electronics	PA2747NL	$61\mu H$ $7A$	
23	1	R1	N/A	N/A	DNP	0805
24	3	R2 R25 R31			330Ω	0805
25	1	R3	Vishay Dale	CRCW0805470RFKEAC	470Ω	0805
26	12	R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15	Vishay Dale	CRCW0805200RFKEA	200Ω	0805
27	4	R16 R17 R18 R19	Stackpole Electronics	RNCP0805FTD10K0	$10k\Omega$	0805

#	Qty	Ref Des	Manufacturer	Mfg Num	Description	Pkg
28	1	R20			$4.7k\Omega$	0805
29	2	R21 R22	Vishay Dale	CRCW08052K20FKEAC	$2.2k\Omega$	0805
30	2	R23 R24			100Ω	0805
31	1	R26			$5k\Omega$	0805
32	4	R27 R28 R29 R30	Vishay Dale	WSLP1206R0250FEA	Shunt $25m\Omega$	1206
33	1	SW1	Panasonic El. Comp.	EVP-BT6A4A000	Push button	
34	1	U1	Analog Devices	MAX865EUA+	Charge pump IC	8-TSSOP
35	1	U2	Analog Devices	LT1991IDD#PBF	Precision OpAmp	10-WFDFN
36	3	U3 U4 U5	Broadcom Limited	ACPL-847-300	Optocoupler	16-SMD
37	1	U7	Microchip	AVR128DB48	AVR 8 bit microcontroller	44-TQFP
38	2	U8 U9	Analog Devices	MAX3441EASA+	RS-485 Transceiver	8-SOIC
39	1	U10	Nexperia	TL431BCDBZR,215	VRef Shunt	SOT-23-3
40	2	LED1 LED2	Würth Elektronik	150060GS75000	Green status LED	0805

Table D.1: Monitor board bill of materials

#	Qty	Ref Des	Manufacturer	Mfg Num	Description	Pkg
1	7	C1 C2 C3 C4 C5 C6 C7	KEMET	C1206C104K5RAC7210	$100nF$ $50V$	1206
2	14	J1 J2 J3 J4 J5 J6 J7 J8 J9 J10 J11 J12 J13 J14	HARTING	09062152821	DIN-41612 H15	
3	1	J15	WAGO	2604-1103	PCB terminal block	
4	1	J16	WAGO	2604-1104	PCB terminal block	
5	7	L1 L2 L3 L4 L5 L6 L7	KEMET	SCT19XV-300-1R9A003JV	30A Common mode choke	
6	7	R1 R2 R3 R4 R5 R6 R7	Vishay Dale	CRCW12061M00FKEAC	$1M\Omega$	1206

Table D.2: Backplane bill of materials